

# RDS+ ROUTER DELAY SIMULATOR



## FEATURES AND BENEFITS

- ✓ Bi-directional independent delay buffers per channel, Full Duplex
- ✓ Supports Split Delays
- ✓ Interfaces supported DS3, E3, STS-1, DS1/E1, TTL, HSSI, RS-232, RS-422/449, RS-530, V.35, and X.21
- ✓ Data Rates: 1.2K to 51.84Mbps
- ✓ Network Simulation Delays of 5mS up to 4 Seconds in 1mS increments, each data path
- ✓ Random Error insertion from  $1 \times 10^{-1}$  to  $1 \times 10^{-12}$  BER
- ✓ Burst Error insertion
- ✓ BERT 511 generator and tester
- ✓ Timing Internal or from either port interface. Accepts external clock for synchronization of internal timing
- ✓ Managed via serial port or web enabled GUI interface
- ✓ Status LED's for each port allows ease of connection and trouble shooting
- ✓ Internal 90-240 VAC auto sensing power supply
- ✓ Sturdy Metal Enclosure



## DESCRIPTION

The Router Delay Simulator Plus (RDS+) allows users to test/stage critical DCE or DTE equipment for reliable network operation while simulating network delay times. The RDS+ provides a realistic simulation of physical network behavior with respect to time delays and bit errors. It supports user circuit rates up to OC-1 (51.84 Mbps) while providing delays from zero to a maximum of 8 seconds round trip. Both continuous random and burst errors are supported.

By using the RDS+ in place of or in series with a real data link (WAN) a wide variety of error conditions can be introduced under controlled and testable conditions.

The RDS+ has two data port interfaces that support EIA-644(LVDS), RS-232, RS-422/449, RS-530, V.35, X.21, DS1/E1, TTL, HSSI, DS3, E3, or STS-1. The data interfaces can be mix and matched where applicable, such as V.35-to-RS-530 connection.

Data Clocking can be driven from various sources. It can be provided via the TX and/or RX clocks of the various data port interfaces. Clocking can also be provided from a programmable clock generator internal to the RDS+. An independent external timing source can be used to frequency-lock the internal timing generator via an external timing port on the back of the RDS+.

Data/Control-Lead Delay is programmable in either seconds or number of data bits. Delay may be specified independently to any value on each of the two bi-directional data paths. An option exists to include a control lead on some interfaces with the data delay.

The RDS+ can introduce Random and/or Burst errors into the data stream. These two error types can be used independently or in a combined fashion. The Random error rate is entered as a range of  $1 \times 10^{-1}$  to  $1 \times 10^{-12}$  errors per bit. Burst errors are entered as duration and interval. The error burst duration is from 1ms to 4 seconds and the interval between bursts is from 1ms to 16seconds. The type of error introduced can be the compliment of the data bit, a forced 0, or a forced 1.

The RDS+ contains one BERT generator and one BERT tester. The generator and tester can be independently attached to either data port. When activated the BERT generator replaces the assigned data port data with a standard  $x^9+x^5+1$  polynomial function to generate a pattern of 511 bits in length. When activated the BERT tester can monitor the data port in either a continuous or a windowed mode. The continuous mode is manually re-triggerable. The windowed mode can be set for a monitor window from 1 to 256ms.

The RDS+ supports digital loopback of either data port. Loopback, Data Delay, Error Simulation, and BERT can all be used simultaneously on a given port. Installation and operation is provided via an operator console port. This port is a RS-232 port that has been tailored for use with HyperTerminal that comes standard with most PCs. RDS+ status and configuration is displayed in real time via this interface. An optional 10Base-T web enabled GUI interface is available for the RDS+.

**EAST COAST DATACOM, INC.**

## SPECIFICATIONS

<b>Application</b>	Interconnection of two devices, (e.g. terminal, modem, or other network or CPE with standard serial digital interfaces) located within proximity of each other while simulating clock generation, network delays, random and burst errors, and BERT capability	
<b>Simulation Delay Times</b>	5 milliseconds(mS) to over 4000 mS, in 1 mS increments, or from 4 bits to over 65,000 bits in 1 bit increments. 4 seconds each data path, 8 seconds round trip delays.	
<b>Capacity</b>	Two (2) data port interfaces	
<b>Data Rates</b>	From 1.2K to 51.84Mbps, user selectable inputs via command prompt or GUI interface.	
<b>Data Port Interfaces</b>	Available in EIA-644(LVDS), RS-232, RS-422/449, RS-530, V.35, X.21, TTL, HSSI, DS1/E1, DS3, E3, STS-1	
<b>Clock Sources</b>	Internal, Stratum 4 or Locked to External, Data Port RX/TX supplied	
<b>Data Format</b>	Synchronous or Asynchronous	
<b>Delay Units</b>	Specified in milliseconds or in bits	
<b>Random Error Rates</b>	From $1 \times 10^{-1}$ to $1 \times 10^{-12}$	
<b>Burst Errors</b>	Burst duration from 1mS to 4 Seconds Off-interval from 1mS to 16 Seconds	
<b>Test Modes</b>	Loopback, 511 BERT	
<b>Operator Console</b>	RS-232 Async, 38.4kbs, (HyperTerminal recommended) *Optional web enabled GUI interface	
<b>Indicators</b>	Power TXD, RXD, TXC, RXC, RTS, CTS, DSR/DTR, DCD for each user port	
<b>Power Source</b>	90-240VAC @10%, 50/60Hz, IEC Power Inlet, (2) 5mm Fuses	
<b>Environmental</b>	Operating Temperature....32° to 122° F (0° to 50° C) Relative Humidity.....5 to 95% Non-Condensing Altitude.....0 to 10,000 feet	
<b>Regulatory Approvals</b>	UL 60950-1:2003, CAN/CSA-C22.2 No. 60950- 1:2003, FCC Part 15, EN55022:2006, ICES-003, Class A	
<b>Dimensions</b>	Height: 1.75 inches (4.44 cm), Width: 17 inches (43.18 cm), Length: 9 inches (22.86 cm)	
<b>Weight</b>	4.5 pounds (2.1 Kg)	
<b>Warranty</b>	Three years, Return to Factory	
<b>Ordering Information</b>	Part #: 175000 Model: RDS-PLUS, Base Unit Description: Router Delay Simulator - Plus	Part #: 175030 Model: RDS-PLUS, GUI Description: Web enabled GUI interface

Interfaces Available	PART #	PRODUCT NAME	TTL TO DIGITAL INTERFACE MODULES
	129014	RS-232 DCE I/M	RS-232, DB-25 Female, DCE Interface Module(connects to DTE)
	129032	RS-232 DTE I/M	RS-232, DB25 Male, DTE Interface Module(connects to DCE)
	129010	V.35 DCE I/M	V.35, MR-34 Pin Female, DCE Interface Module(connects to DTE)
	129028	V.35 DTE I/M	V.35, MR-34Pin Male, DTE Interface Module(connects to DCE)
	129011	RS-530 DCE I/M	RS-530, DB-25 Female, DCE Interface Module(connects to DTE)
	129029	RS-530 DTE I/M	RS-530, DB-25 Male, DTE Interface Module(connects to DCE)
	129012	RS-422 DCE I/M	RS-422/449, DB37 Female, DCE Interface Module(connects to DTE)
	129030	RS-422 DTE I/M	RS-422/449, DB-37 Male, DTE Interface Module(connects to DCE)
	129013	X.21 DCE I/M	X.21, DB-15 Female, DCE Interface Module(connects to DTE)
	129031	X.21 DTE I/M	X.21, DB-15 Male, DTE Interface Module(connects to DCE)
	129057	TTL I/M	TTL Interface Module W/BNC Connectors
	129085	T-1 I/M	T-1 Interface Module, 1.544 Mbps, DB-15 Female
	129097	E-1 I/M	E-1, G.703 Interface Module, 2.048 Mbps, 75 ohm BNC
	151028	HSSI DCE I/M	HSSI, SCSI-I 50 Pin Female, DCE Interface Module(connects to DTE)
	175020	DS3 I/M	DS3 Interface Module, 44.736 Mbps, 75 ohm BNC
	175021	E3 I/M	E3 Interface Module, 34.368 Mbps, 75 ohm BNC
	175022	STS-1 I/M	STS-1 Interface Module, 51.840 Mbps, 75 ohm BNC
	175040	EIA-644(LVDS)	EIA-644(LVDS), DCE Interface Module, DB-25 Female, 52Mbps
	175045	EIA-644(LVDS)	EIA-644(LVDS), DTE Interface Module, DB-25 Male, 52Mbps

# OVERVIEW: RDS-PLUS GUI OPTION W/DEDICATED IP ADDRESS

EAST COAST DATACOM, INC. RDS+

RS-232 DCE RS-232 DCE

PowerOn Config PUSH FOR I.P. ADDRESS ROUTER DELAY SIMULATOR PLUS

Save Load Submit Cancel **BERT Tester**

## NETWORK DELAY SIMULATOR PLUS

Firmware 1.01.0  
 FPGA 1.00  
 IPadr: 192.168.1.100  
 IPmask: 255.255.255.0  
 Gateway: 192.168.1.0

Tester Off  
 Enabled on PortA to PortB path  
 Enabled on PortB to PortA path  
 Window with size of  bits  
 Continuous (1-1677215)

Error Count  [Clear Count](#)

**PORT A to PORT B Path >>** RXC=64 KHz TXC=64 KHz

<p><b>Data Source A</b></p> <p><input checked="" type="radio"/> No Delays</p> <p><input type="radio"/> <input type="text" value="5"/> ms delay (5-4095)</p> <p><input type="radio"/> <input type="text" value="16"/> bit delay (16-65535)</p> <p><input type="radio"/> BERT 511 generator</p> <p><input type="checkbox"/> Loopback from PortB</p> <p>Working Data Clock Range: <input type="text" value="1200bps"/></p> <p><input type="checkbox"/> Delay Control with Data</p>	<p><b>Burst Errors</b></p> <p><input type="text" value="1"/> Duration (1-4095ms)</p> <p><input type="text" value="1"/> Interval (1-16383ms)</p> <p><input type="text" value="Compliment Bit"/> Type Error</p> <p><input type="text" value="n=0"/> Error Rate 1x10<sup>9</sup></p>	<p><b>Random Errors</b></p> <p><input type="text" value="Compliment Bit"/> Type</p> <p><input type="text" value="n=1"/> Error Rate 1x10<sup>9</sup></p> <p><a href="#">Create Single Bit Error</a></p>
---	---	--

**PORT B to PORT A Path <<** TXC=64 KHz RXC=64 KHz

<p><b>Data Source B</b></p> <p><input checked="" type="radio"/> No Delays</p> <p><input type="radio"/> <input type="text" value="5"/> ms delay (5-4095)</p> <p><input type="radio"/> <input type="text" value="16"/> bit delay (16-65535)</p> <p><input type="radio"/> BERT 511 generator</p> <p><input type="checkbox"/> Loopback from PortA</p> <p>Working Data Clock Range: <input type="text" value="1200bps"/></p> <p><input type="checkbox"/> Delay Control with Data</p>	<p><b>Burst Errors</b></p> <p><input type="text" value="1"/> Duration (1-4095ms)</p> <p><input type="text" value="1"/> Interval (1-16383ms)</p> <p><input type="text" value="Compliment Bit"/> Type Error</p> <p><input type="text" value="n=0"/> Error Rate 1x10<sup>9</sup></p>	<p><b>Random Errors</b></p> <p><input type="text" value="Compliment Bit"/> Type</p> <p><input type="text" value="n=1"/> Error Rate 1x10<sup>9</sup></p> <p><a href="#">Create Single Bit Error</a></p>
---	---	--

**Data Clock Sources** (Note: Check-boxes in front of the clock selections below are used to invert the clock.)

Internal Clock:

<input type="checkbox"/> Port A RX CLK ← <input type="text" value="Internal"/>	<input type="checkbox"/> Buff In CLK <input type="text" value="Internal"/>	<input type="checkbox"/> Port A to Port B Buffer<> <input type="text" value="Internal"/>	<input type="checkbox"/> Buff Out CLK <input type="text" value="Internal"/>	<input type="checkbox"/> Port B TX CLK → <input type="text" value="Internal"/>
<input type="checkbox"/> Port A TX CLK ← <input type="text" value="Internal"/>	<input type="checkbox"/> Buff Out CLK <input type="text" value="Internal"/>	<input type="checkbox"/> Port B to Port A <<Buffer <input type="text" value="Internal"/>	<input type="checkbox"/> Buff In CLK <input type="text" value="Internal"/>	<input type="checkbox"/> Port B RX CLK → <input type="text" value="Internal"/>
<input type="checkbox"/> Port A TXCE CLK →	<input type="checkbox"/> Enable External Reference Clock with divisor of <input type="text" value="1"/> (1-256)			<input type="checkbox"/> Port B TXCE CLK ←

The following RTS/CTS delays are only applicable when both ports are DCE.

Port A RTS/CTS delay   
 Port B RTS/CTS delay

Page Refresh Rate

**EAST COAST DATACOM, INC.**  
 245 Gus Hipp Boulevard, STE 3  
 Rockledge, FL 32955-4812 U.S.A.  
**WEB SITE: www.ecdata.com**

TEL: (321) 637-9922

FAX: (321) 637-9980

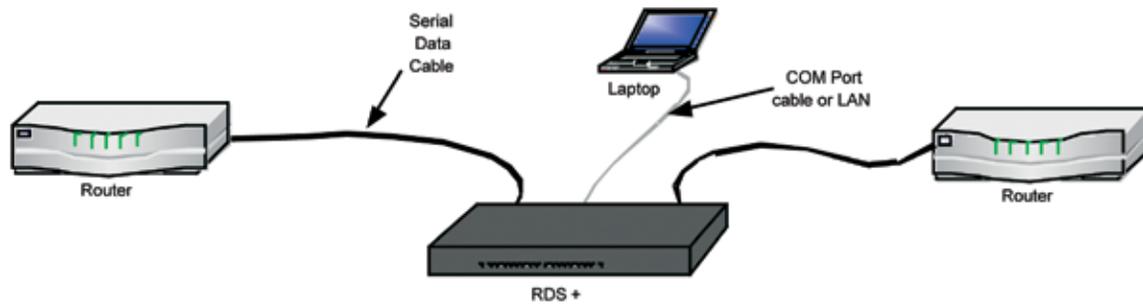
## OVERVIEW: RDS-PLUS W/SERIAL PORT CONNECTION AND OPERATION

The RDS+ has a Power LED, one System Status LED and a set of status LED's for each Port interface, which allow the user to visually confirm the presence of data and clock, and certain control or status signals. The RDS+ is designed with state of the art digital CMOS technology.

The RDS+ is housed in a sturdy 1U high metal enclosure which can be rack mounted. It is powered by an integrated 90-240V 50/60Hz power supply. The RDS+ has a one year warranty and a 24 hour turnaround on warranty repairs.

### Typical Simulation Example

Figure 1 illustrates a common example of utilizing the RDS+ between a pair of high-speed routers in a staged network to simulate the actual network conditions with respect to delays and potential line errors. In this example the RDS+, which has the capability to synthesize all standard telecom clocks, provides interface clocking to both routers. Using a computer, such as a laptop running HyperTerminal, an operator is able to adjust delay and error settings for various networking scenarios and test setups.



Simulating Network Conditions Between 2 Routers

### Other Network Simulations and RDS+ Uses

The RDS+ is capable of performing in configurations other than the previous example. Some of the possible uses may include the following:

- 1) Simulating the delays and transmission impairments of geosynchronous satellite networks
- 2) Measuring error recovery performance of DTE when inserted between a modem and DTE
- 3) Modeling number-of-bit delays to simulate buffer and queue effects
- 4) Buffering between clock sources with long-term cyclic drift (e.g. Doppler effect), where delay is not critical
- 5) Simulating long-haul terrestrial transmission delays

### Internal Clock Timing

Internal Clock Timing is normally used when both RDS+ interface cards are DCEs. In this configuration, clocks are sent from the RDS+ to both attached devices. The internal clock source is a Stratum 4 standard clock when it runs without an external timing source. An external timing source may be used with the internal oscillator to frequency-lock the generated internal clocks to an external reference. The external reference must be a multiple of 8KHz, within 100 ppm of nominal frequency, up to a maximum of 2.048 Mbps.

### Flow-through Clock Timing, Unidirectional and Bidirectional

Flow-through Timing allows one attached device to clock the RDS+, and to pass that clock timing to the other attached device. Typically, the RDS+ will have one DCE and one DTE to facilitate this configuration. In this application, the internal clock will not be used. With the flexibility of assigning and routing interface clocks on the RDS+, the clock timing flow may be either bidirectional or unidirectional. Unidirectional works best when both cards are standard EIA-type interfaces, where one is a DTE and receives a transmit and receive data clock, and the other is a DCE which sends a transmit and receive data clock. In this case the timing flow is from DTE to DCE.

Bidirectional timing flow is usually associated with interface types that have a receive clock and a transmit clock that travel in the same direction as the corresponding data signal. This is typical of DS-1, DS-3, and the TTL Interface Card. Timing usually passes through the RDS+ in the same direction as the data. Since the data is bidirectional, then so is the clocking. With bidirectional timing it is also not required that the two clock signals in opposing directions have the same frequency (split speed).

### Independent Clock Timing

When both interface cards are DTE, then they both must accept timing from an attached device. It is possible to use the RDS+ in such a configuration, but it is important that the user must be able to insure that the separate clocks are timed to the same clock source, otherwise the delay buffer will not provide constant delay.

There are also applications where the RDS+ delay buffer may be used as an elastic storage buffer, where the two independent clock sources are timed differently. In this case the delay through the buffer is not constant, but variable over time.

## EAST COAST DATACOM, INC.

245 Gus Hipp Boulevard, STE 3  
Rockledge, FL 32955-4812 U.S.A.

WEB SITE: [www.ecdata.com](http://www.ecdata.com)

TEL: (321) 637-9922

FAX: (321) 637-9980