

OPERATIONS MANUAL

RDS-PLUS

Advanced Network/Router Delay and Error Simulator

3 JAN 2012

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1 Introduction.....	3
1.1 Typical Simulation Example	3
1.2 Other Network Simulations and RDS+ Uses	3
2 Functional Description	4
2.1 Feature Summary	4
2.2 System Capabilities.....	5
2.2.1 System Diagram.....	5
2.2.2 Data Flow	6
2.2.2.1 Data Path and Delay Buffer Interface	7
2.2.2.2 Error Event Generators	9
2.2.2.3 BERT	10
2.2.2.4 Data Path Loops.....	10
2.2.2.5 Control Lead Routing	10
2.2.3 Timing and Clocks.....	11
2.2.3.1 Clock Selection and Timing Functions	11
2.2.3.2 External Timing	12
2.2.4 Indicators.....	12
2.2.5 Management Interfaces	12
2.2.5.1 Async Terminal Management Port.....	12
2.2.5.2 LAN Management Port.....	12
2.3 Physical Characteristics	12
2.3.1 AC Mains Power	13
2.3.2 Thermal requirements	13
3 User Interface	14
3.1 Front Panel Indicators	14
3.2 Console Operation	14
3.2.1 Console Setup.....	15
3.2.2 Start-Up and Session Initiation	15
3.2.3 Operator's Display Window Status Area.....	16
3.2.4 Operator's Display Window Menu Area	18
3.2.5 Menu Screens and Navigation	18
3.2.5.1 Menu Tree	18
3.2.5.2 Top-Level System Menu	18
3.2.5.3 Configuration Save/Restore	20
3.2.5.4 Port Configuration	21
3.2.5.5 Clock Options	22
3.2.5.6 Data Path Delays	22
3.2.5.7 Error Insertion.....	23
3.2.5.8 BERT	24
3.2.5.9 Data Loop.....	25
3.2.5.10 LED Display.....	26
3.2.6 System Monitor Screen.....	27
3.2.6.1 Firmware Download Procedure.....	27
3.3 HTML Browser Access via LAN	28
3.3.1 Getting Started	28
3.3.2 RDS+ Web Page Interface.....	30
A Questions, Common Problems and Helpful Tips.....	31
A.1 Differences between Simulated Delay and Real Delay	31

A.2	Types of Working Configurations	32
A.2.1	Internal Clock Timing	32
A.2.2	Flow-through Clock Timing, Unidirectional and Bidirectional	32
A.2.3	Independent Clock Timing	32
A.3	Interfaces with Clock and Data Recovery (DS-1, E1, DS-3, E3, STS-1).....	32
B	Port Interface Cards	34
B.1	Strapping Charts	34
C	System Information	36

SAFETY WARNING

Always observe standard safety precautions during installation, operation and maintenance of this product. To avoid the possibility of electrical shock, be sure to disconnect the power cord from the power source before you remove the IEC power fuses or perform any repairs.

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Introduction

The RDS+ is a modular, network link error and delay simulator that provides a realistic simulation of physical network behavior with respect to time delays and bit errors. The RDS+ supports a wide range of interface types and speeds, ranging from 1200bps to over 50Mbps.

Simulated network delays are bi-directional, independently controlled and may be set from 5mS up to 4 seconds in length.

A variety of error conditions can be introduced under controlled and testable conditions. Both continuous random and burst errors are supported.

1.1 Typical Simulation Example

Figure 0-1 illustrates a common example of utilizing the RDS+ between a pair of high-speed routers in a staged network to simulate the actual network conditions with respect to delays and potential line errors. In this example the RDS+, which has the capability to synthesize all standard telecom clocks, provides interface clocking to both routers. Using a computer, such as a laptop running HyperTerminal, an operator is able to adjust delay and error settings for various networking scenarios and test setups.

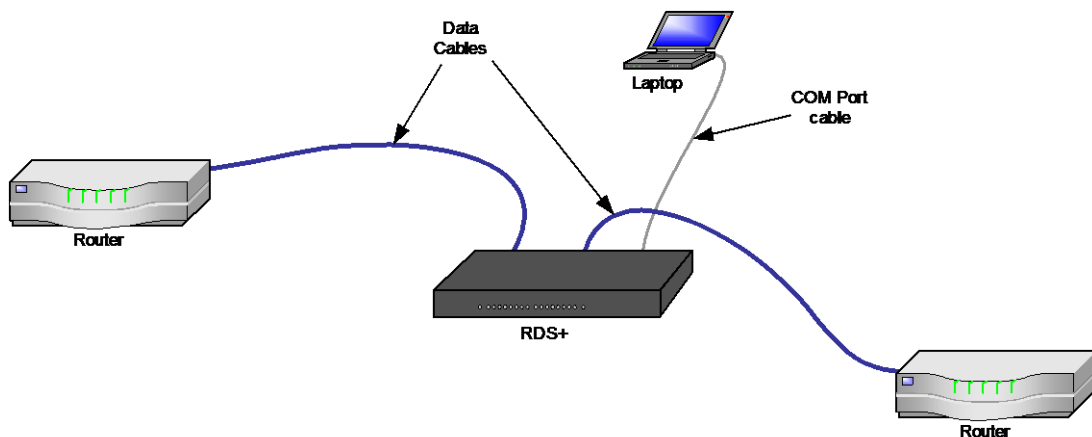


Figure 0-1 Simulating Network Conditions Between 2 Routers

1.2 Other Network Simulations and RDS+ Uses

The RDS+ is capable of performing in configurations other than the previous example. Some of the possible uses may include the following:

- 1) Simulating the delays and transmission impairments of geosynchronous satellite networks.
- 2) Measuring error recovery performance of DTE when inserted between a modem and DTE.
- 3) Modeling number-of-bit delays to simulate buffer and queue effects.
- 4) Buffering between clock sources with long-term cyclic drift (e.g. Doppler effect), where delay is not critical
- 5) Simulating long-haul terrestrial transmission delays.

2 Functional Description

This section presents the functional operation and concepts of the RDS+. Readers should familiarize themselves with this section before proceeding to the Hardware Installation section.

2.1 Feature Summary

The prominent features of the RDS+ are outlined in the following table:

<p>Delay Simulators</p> <ul style="list-style-type: none">2 independent buffers, one for each data directionTime delay programmable from 5mS to 4 seconds, over all ratesBit delay programmable from 33 bits to 65538 bits, over all rates <p>Error Simulators</p> <ul style="list-style-type: none">2 independent Random Error simulators, and 2 independent Burst Error simulatorsRandom error simulator variable from 1×10^{-1} to 1×10^{-12}Burst error simulator variable from 1×10^{-1} to 1×10^{-3}, with on intervals programmable from 1mS to 4 sec., and off intervals programmable from 1mS to 16 sec. <p>Data Rates</p> <p>Data rates supported for all port interface options and synthesized clocks from 1200bps to 51.84Mbps</p> <p>Internal synthesizer produces virtually all common data and telecom clock rates in above range</p> <p>1200; 1800; 2400; 3600; 7200; 9600; 14.4K; 19.2K; 28.8K; 38.4K; 57.6K; 115.2K</p> <p>16K; 32K; 56K; 64K; 128K; 192K; 256K; 384K; 512K; 768K; 1024K; 1344K; 1472K; 1536K; 1544K; 1920K; 1984K; 2048K; 3072K; 4096K; 6144K; 6176K; 10M; 25M; 34.368M; 44.736M; 50M; 51.840M</p> <p>BERT Tester</p> <ul style="list-style-type: none">Independent 511 Pattern generator and checker, assignable to either data path.Data Loop modes to facilitate BERT self-testing <p>Port Interfaces</p> <ul style="list-style-type: none">Available optional plug-ins: RS-232, RS-422/449, RS-530, V.35, X.21, TTL, HSSI, DS1/E1, DS3, E3, STS-1External Clock: Single-ended RS-423 or TTL; differential RS-422, RS-485, or similarConsole Port: RS-232 DCE, DB-9 female <p>Clocking Options</p> <ol style="list-style-type: none">1) Internal Synthesizer (Stratum 4);2) External Clock port (rate = $n \times 8\text{KHz}$, $n = 1$ to 256) frequency-locks internal synthesizer;3) Any incoming port interface clock <p>System Features</p> <ul style="list-style-type: none">Down-line loading of firmware revisionsLocal non-volatile storage and retrieval of factory and user configurations

Table 1 – RDS+ Prominent Features

2.2 System Capabilities

The RDS+ is comprised of dedicated and programmable hardware, along with a processor-based firmware operating system. Together with optional port interface modules, and an external user-provided terminal, the product supports all the functions described in this document.

2.2.1 System Diagram

The diagram of Figure 2-1 depicts the functional hardware elements of the RDS architecture. In this architecture, the Microprocessor, SRAM, and FLASH Memory along with the Management (MGT) ports and the Front Panel support the user interface and system management functions.

The FPGA, the SDRAM, and the Port A and B option cards provide the data path hardware functions, and the direct system interfaces to control and monitor those functions and the timing functions.

The External Timing port and the Clock Generation block provide all timing for the data path elements.

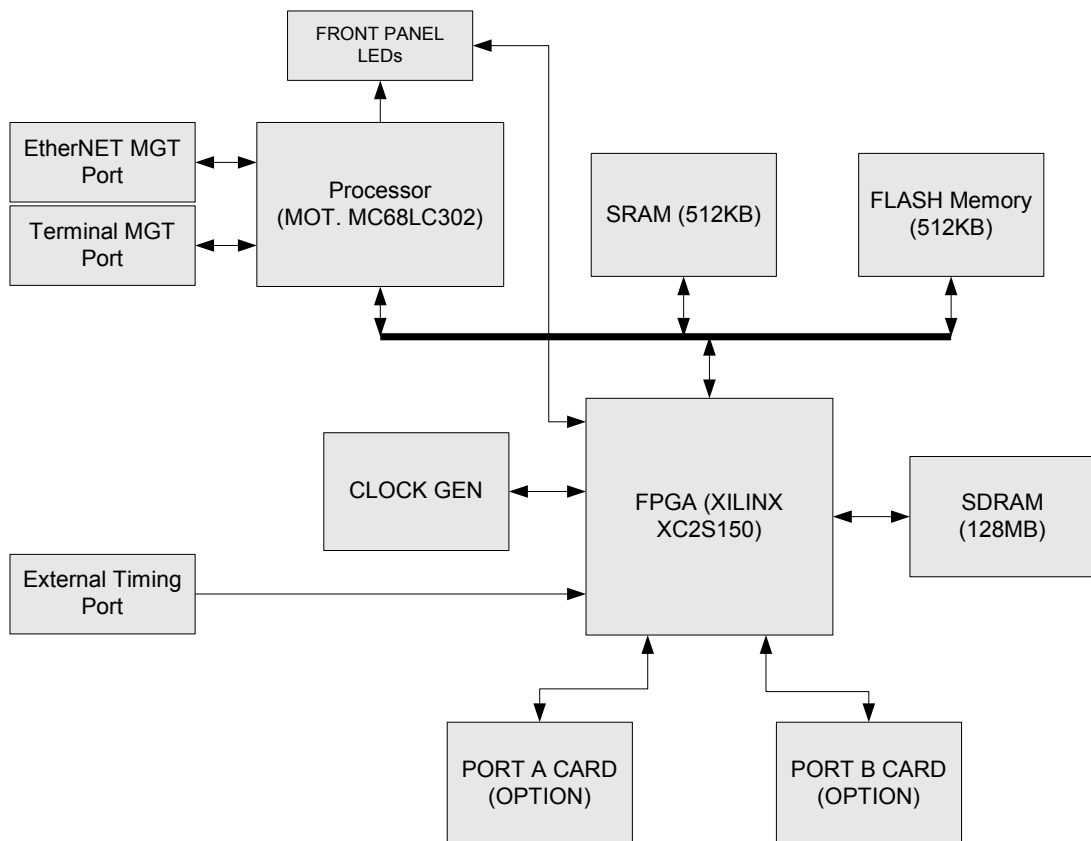


Figure 2-1 – RDS+ System Hardware Diagram

2.2.2 Data Flow

A general diagram of the data path functions and data flow is depicted in Figure 2-2. Data paths are defined in terms of the path from Port A to Port B (Data Path 1) and Port B to Port A (Data Path 2). All functions may be applied equally to either data path. Some resources are duplicated in each path, while others serve the entire system, but may be selected to perform their function on either path.

Since both data paths are symmetrical, the following description of path 1 applies equally to path 2:

Incoming bit-serial data and one control signal (e.g., RTS) from Port A, as well as Loop data from Path 2 are presented to the input to the Data Path 1 block. All data and control signals are synchronized to an input clock selected in the Port and Buffer Clock Routing block.

The Data Path 1 block controls the steering of port and loop data, buffered delay data, random and burst error events, and BERT pattern data to produce the selected functions on the output data stream. This block is also responsible for formatting parallel data for writing into the SDRAM buffer, recovering serial data upon reading, and generating the appropriately timed memory access requests and addresses to the SDRAM Access Arbiter.

The SDRAM Access Arbiter and Refresh Controller handles the interleaving of memory read/write requests from the Data Path 1&2 blocks along with periodic memory refresh timer requests. It is also responsible for proper initialization of the SDRAM on power-up.

Each data path has a dedicated Random Error Generator and Burst Error Generator. These blocks are independently controlled and may be selected to work in tandem.

The system has one BERT Pattern Generator and one BERT Pattern Checker. Each may be independently enabled, as well as the data path to which they are applied. The BERT Pattern used is a standard 511 pattern, using a generator polynomial of x^9+x^5+1 .

The Clock Generation and Control block is used to generate an optional selectable internal data rate clock based upon the internal 24.576MHz oscillator. This oscillator is part of a Phase-Locked Loop (PLL) signal generation circuit that is able to accept an External Timing Reference. Other time-based signals required by the FPGA for other functions are also generated in this block.

The external reference must be a multiple of 8KHz, with a maximum frequency of 2048 KHz. Without an external reference the internal oscillator will operate within Stratum 4 specifications.

All port data clock selection is managed via the Port and Buffer Clock Routing block. Each pair of buffer clocks and each outbound interface clock may be individually selected, and optionally inverted through this logic. Selectable input clocks to this block include the output of the Clock Generation and Control block, and the input transmit and receive clocks from each Port Interface, depending on the type of interface used.

The Control and Status Register block encompasses all the microprocessor-accessible registers used to configure or control the FPGA, or to obtain operational status.

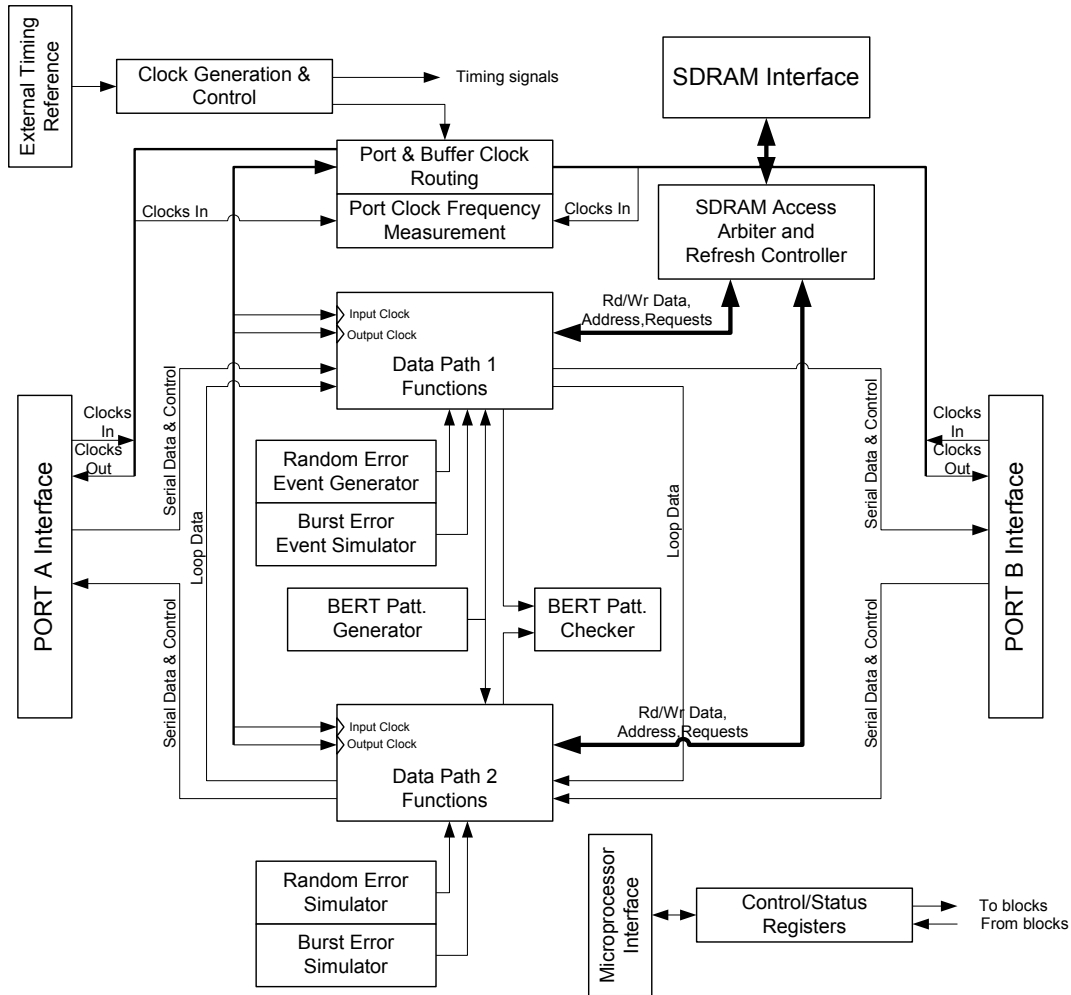


Figure 2-2

2.2.2.1 Data Path and Delay Buffer Interface

Figure 2-3 shows a more detailed view of the Data Path 1 Functions block, including its interface to the SDRAM Access Arbiter and Refresh Controller (SDRAM Controller), which forms the Delay Buffer.

The data path is controlled through a series of multiplexers and steering logic from which a serial data stream emerges. Inputs include serial data from Port A, serial loop data from Path 2, a control lead from Port A, and the outputs of the BERT Pattern Generator, the Random Error Event Generator, and the Burst Error Event Generator.

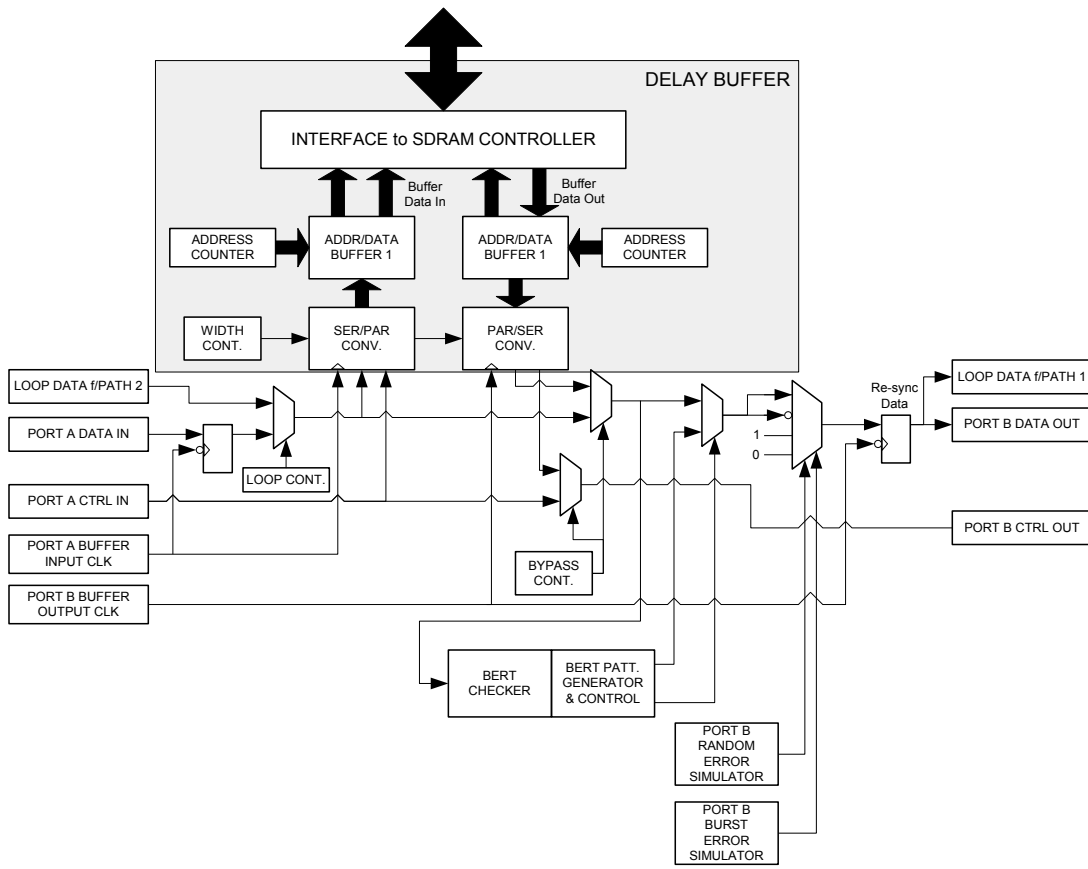


Figure 2-3

2.2.2.1.1 Delay Buffer

The interface to the SDRAM Controller includes logic between the first and second multiplexers to break the data path and insert delay. The Delay Buffer may be bypassed, but when enabled, serial data, and optionally the control lead, are formatted and stored in sequential locations in memory. At a later time defined by the delay parameter, the same information is read from memory, unformatted and presented to the second multiplexer, forming the delayed data stream.

When using the Delay Buffer, data is clocked in with the Port A Buffer Input Clock. This data is assembled into a serial-to-parallel converter to take efficient advantage of the memory bandwidth. The size of the serial word depends on the data rate.

For low speed data, the data word is only one or two bits wide. This helps to minimize the buffer latency and permit small delay increments, especially when the delay is being specified in bits rather than time. It also helps to more closely align control lead changes on output to the bit period during which they occurred on input.

For high-speed data the word may be up to 16 bits wide. This is required to achieve bit rates of up to 52Mbps, where buffer latency and resolution become insignificant errors in delay time as a result of the higher speed data clock.

The Delay Buffer determines delay by initiating write cycles to the SDRAM as soon as the delay function is enabled. The starting address for the write operations is address zero, the first physical location in memory. Writing continues in sequential address locations as long as the delay is enabled and an input clock signal is present.

Read cycles start only after the delay period has elapsed when operating in a time delay mode, or only after a specified number of bits has been received and stored when operating in a bit delay mode. The starting address for read operations is also address zero.

Both read and write addresses count upwards through memory, with the write address being “ahead” of the (delayed) read address. When the last physical location in memory is reached, the address counter returns to zero and begins counting upwards again.

In this way, delay is simulated. It should be clear that a constant delay depends on a clock of identical and constant frequency at both buffer input and buffer output, otherwise the actual delay will be affected. Cases where different clocks are selected as buffer input clock and buffer output clock may exist, but in most applications they are the same.

NOTE: Time delay and bit-delay parameters are different methods of expressing delay, but the underlying principles of delay buffer operation are identical. As long as the buffer input and buffer output clock rates are identical, the number of bits stored in the buffer at any given time remains constant. Changing the rate of the buffer clocks results in proportional changes in buffer delay, while the number of bits does not change. This is because the change in clock rate will alter the time interval of each bit entering or leaving the buffer. In general, it is not advised to alter clock rates while the delay buffer is in operation, unless the user is thoroughly familiar with the concepts of delay buffer operation.

2.2.2.2 Error Event Generators

Both Error Event Generators are based on an array of pseudo-random number generators working in a scalable configuration to produce a near-Gaussian distribution of error events with the specified BER. Error events are defined as one-bit in length.

The Burst Error Event Generator differs from the Random Error Event Generator in that it produces randomly distributed errors only within confined periodic windows, called bursts.

The action that is created by an error event may be controlled by the user by selecting an error type. Error type options include forcing the affected bit to a one, forcing to a zero, inverting the bit, and leaving the bit unchanged.

Both error generators may be simultaneously enabled, creating the possibility that error events from the two generators may occur in the same bit period. If the error type is the same, then the bit is modified according to that code. If the error type is different, then the error type associated with the Burst Error Event Generator assumes precedence.

2.2.2.2.1 Random Error Event Generator

A BER range of 10^{-1} down to 10^{-12} is supported for the Random Error Event Generator. Error events are produced continuously in a near-Gaussian distribution. Although the error event generators are deterministic rather than truly random, the repetition period is many years in length, even at the highest supported rates.

2.2.2.2.2 Burst Error Generator

Within burst periods, a BER range of 10^{-1} and 10^{-2} is supported. Burst events are defined with duration and interval. The duration of a burst period is that time during which the random errors events are actively being generated. The interval of a burst period is that time during which the error events are disabled, or the time between error bursts.

The burst duration may be set from 1 mS to 4095 mS, in 1 mS increments.

The burst interval may be set from 1 mS to 16383 mS in 1 mS increments.

2.2.2.3 BERT

The BERT logic is a single pattern generator and pattern checker. The pattern used is the standard 511 pattern. The generator produces a continuous 511 pattern that is selectable to be output on either port.

Since the BERT generator insertion point is prior to the error event multiplexers, the error generators may be used to impose a programmable error rate on the 511 pattern.

The BERT checker may be fed from either data path. The logical point that this is done is after the delay buffer and the loop control, but prior to the BERT generator. In this way, the BERT generator and checker may be used to check the entire internal RDS+ FPGA data path simply by enabling both loopbacks, and applying the BERT checker to the same data path as the generator.

2.2.2.4 Data Path Loops

Two Data Path Loop multiplexers are located at the input to each data path in order to source data from the output of the alternate Data Path. Thus the input to Path 1 may be looped from the output of Path 2, and likewise the input to Path 2 may be looped from the output of Path 1.

The looped data is sent to the serial data output lead in a normal fashion.

Since the serial data out of one data path is timed to the buffer output clock of that path, it is important to insure that the clock assigned to the buffer input of the looped-to data path is the same clock, or has a known phase relationship that will capture data reliably.

2.2.2.5 Control Lead Routing

The Data Path Buffer is able to transport one control lead, defined by the type of interface, along with the data, making it subject to the same delay as the data. If this function is not enabled by the user, the control signal bypasses the delay buffer, regardless of whether it is used for data delay or not.

An exception to the above routing of control signals exists when the RDS+ has been configured with two EIA-type DCE port interface modules. In this case only, the CTS control signal is not routed through the buffer from one port to the other, but rather is looped back to the same local port, following the RTS input.

With this configuration, shown in Figure 2-4, the operator may select a programmable delay, Pd, from among several options ranging from zero delay to 200mS delay. The delay of CTS chose in this configuration is independent of the buffer delay for data.

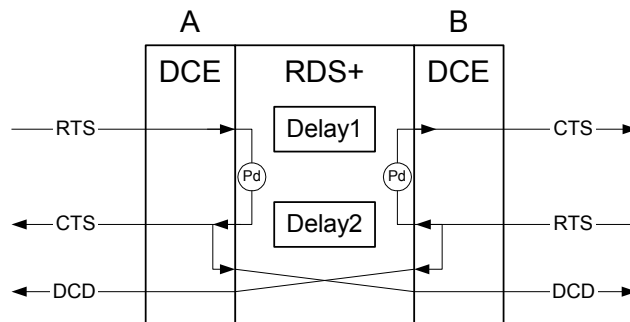


Figure 2-4 – Dual DCE RTS-to-CTS Loop function

2.2.3 Timing and Clocks

2.2.3.1 Clock Selection and Timing Functions

The RDS+ has a very flexible scheme for selecting clocks, both at the buffer input and output, and at the port card interfaces. Figure 2-5 illustrates this for Port A – and identical mirror of this function exists for Port B.

There are four possible external clocks and one internal clock that may be selected.

NOTE: In practice, four distinct external clocks are only present when both Port A and Port B are EIA-type DTE interfaces. Nevertheless, the option is available to select any one of these clocks. When the Port A interface is a DCE, there is still one clock that is available, referred to often as SCTE, TXCE, or TT that will be on the same signal as Port A TX Clock IN.

The internal Clock Generator is the fifth option.

Clocks may be selected independently for each of the two Port A Tx Clock and Rx Clock outputs, when used. Clocks must be selected for the Buffer 1 Input and Buffer 2 Output (these are the sides of the two buffers that are associated with Port A serial data).

It is important to be aware of the serial data timing relationships of each port's transmit and receive data with their respective clocks in order to avoid making clock selections which do not capture data on buffer input or reproduce data alignment on buffer output.

For each of the four clock selections associated with Port A, there are independent controls for the inversion of each clock signal. This option is used most often to compensate for cable delays in configurations in which source timing is not available.

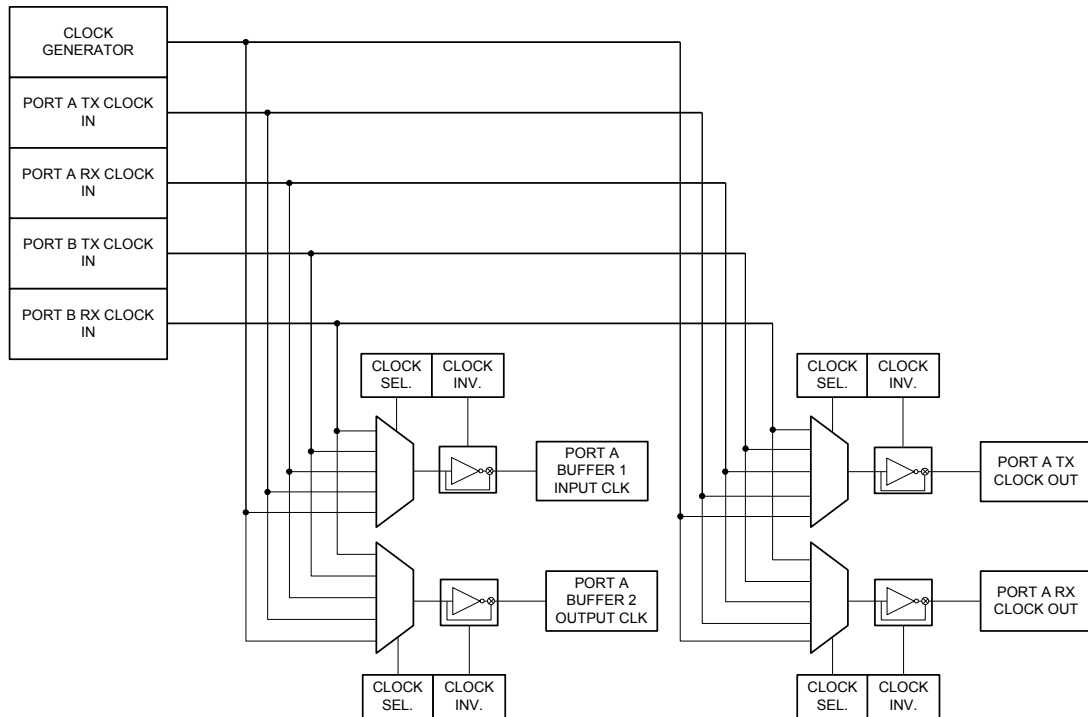


Figure 2-5 – Clock Selection and Routing

2.2.3.2 External Timing

The internal Clock Generator has the ability to be frequency-locked to an optional external timing source. This may be any clock that is equivalent to Stratum 4 accuracy, or better. A less stable clock may also be used, but accuracy must be within +/-50 ppm in order to guarantee it is within the pull range of the internal voltage-controlled oscillator (VCO).

The external clock may be of any nominal frequency that is a multiple of 8KHz, up to a maximum of 2.048 MHz. When applying an external clock, the user must insure that the configuration includes setting the clock divisor to yield an 8KHz reference frequency. For example, if the applied external clock is 1.024 MHz, the divider must be set to 128, i.e., $1,024,000 = 8,000 \times 128$. For an 8 KHz external timing clock, the divisor is set to 1.

2.2.4 Indicators

An array of eighteen LEDs on the Front Panel provide the operator a quick indication of status of the system and port operation. For the system, LEDs provide simply an indication of Power Supply output and a general system operating health indication.

For each port, an identical set of indicators provide information on clock and data activity, and EIA control lead status. When not using an EIA-type port interface card in one of the slots, some of the LEDs associated with control leads may be programmed to reflect other status.

Clock and data LEDs, when ON, represent the signal activity of the data or clock lead they monitor, rather than the state or signal level. Therefore, if a data signal for example, was stuck at high or stuck at low, the corresponding LED would be OFF in either case.

2.2.5 Management Interfaces

2.2.5.1 Async Terminal Management Port

The primary method for user control, configuration and status of the RDS+ is through the Async Terminal Management Port. This port is RS-232 implemented on a DB-9 female connector. A terminal emulation program, in particular HyperTerminal running on a PC, is the best compatible method to utilize this interface and access the firmware application that runs on the RDS+ microprocessor. The user should set HyperTerminal to 38.4kbps, 8,N,1 and no flow control for proper operation.

The firmware utilizes the capabilities of HyperTerminal to present a character-graphic display within the terminal window that is descriptive of the system status while presenting all the available options for configuration and real-time control.

2.2.5.2 LAN Management Port

The purpose of the LAN Management Port is to provide the means to access a resident HTML server via a standard client web browser such as MSIE. This server application provides a more GUI-oriented presentation to the operator without the need for a proprietary PC-based application.

All RDS+ functions available via the Async Management Port are accessible via the LAN Management Port.

2.3 Physical Characteristics

The RDS+ system is housed in a standard 1U high rack-mountable enclosure. Mounting brackets for rack-mounting are optional, as well as rubber feet for bench-top use.

Figure 2-6 and Figure 2-7 show front and rear views, respectively of the RDS+ with important features noted.

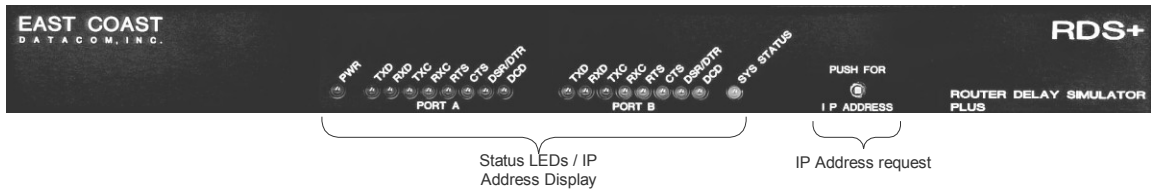


Figure 2-6 – RDS+ Front View

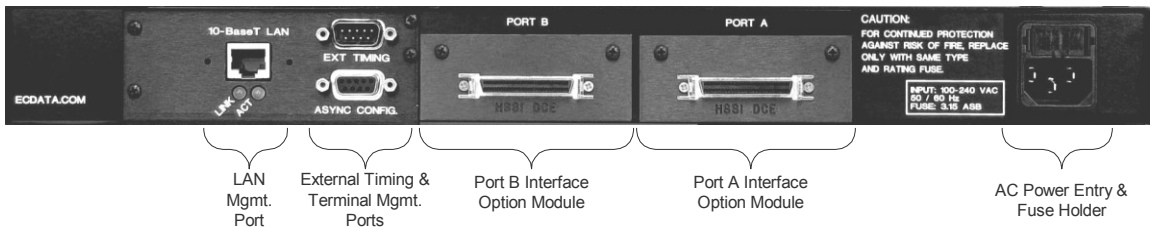


Figure 2-7 – RDS+ Rear View

2.3.1 AC Mains Power

The RDS+ accepts power from 85 to 264 VAC, and from 47 Hz to 63 Hz. Power entry is by means of a standard 3-prong AC line cord with an Earth ground as the 3rd conductor.

NOTE: It is very important that the Earth ground be connected to a suitably grounded outlet.

The IEC Power Entry Module also contains a dual fuse holder. The following fuse ratings are required for proper and safe operation:

- 90 - 250V AC, 50/60 Hz:
- 3.15 Amp, Slow-Blow, Low Clearance, 5mm x 20mm

2.3.2 Thermal requirements

No special or external forced-air cooling is required. The RDS+ chassis is designed to be convection-cooled, provided that the ambient temperature meets the system specification.

3 User Interface

3.1 Front Panel Indicators

The front panel of the RDS+ has a display area with 18 LEDs. These are described in the following list:

PWR –Power indicator (green); when ON indicates that the internal power supply is producing a DC output to power the internal logic circuits.

Port A and Port B (Identical sets of 8 LEDs)

TXD –Transmit Data (green); when ON indicates that there are signal transitions on the logic side of the transmit data lead of the port interface, prior to the line interface circuit.

RXD – Receive Data (green); when ON indicates that there are signal transitions on the logic side of the receive data lead of the port interface, prior to the line interface circuit.

TXC –Transmit Clock (green); when ON indicates that there are signal transitions on the logic side of the transmit clock lead of the port interface, prior to the line interface circuit.

RXC –Receive Clock (green); when ON indicates that there are signal transitions on the logic side of the receive clock lead of the port interface, prior to the line interface circuit.

RTS – Request-To-Send (green); represents the ON/OFF state of the RTS interface lead, if present.

CTS – Clear-To-Send (green); represents the ON/OFF state of the CTS interface lead, if present.

DSR/DTR – Data Set Ready or Data Terminal Ready (green); represents the ON/OFF state of the DSR (if the interface type is a DTE) or DTR (if the interface type is a DCE). If another type of interface is inserted, this LED is normally OFF.

DCD – Data Carrier Detect (green); represents the ON/OFF state of the DCD interface lead, if present.

SYS STATUS – System Status (bicolor: green or yellow); provides an indication of system status and health. Yellow indicates the system is initializing, normally following a reset or power-up. If boot and initialization complete properly, the LED is changed to Green. If this LED is OFF, and the PWR LED is ON, a system hardware failure has occurred.

3.2 Console Operation

Managing the operation, configuration and status of the RDS+ requires the connection of PC-based terminal emulation program (HyperTerminal) via the Console Port. Through the

terminal interface, the user is presented a character-graphic display window with a series of hierarchical menus through which options are selected.

3.2.1 Console Setup

The Console Port of the RDS+ has hardware interface characteristics as shown in the following table, which should be noted when configuring HyperTerminal:

Elec. Interface	RS-232, DCE
Timing	38,400 bps
Connector	DB-9, Female
Format	Async, 8bit data, No parity, 1Stop bit
Flow Control	None

Table 2 – Console Terminal Interface Settings

Additionally, the RDS+ console interface is designed to echo characters as they are received from the terminal, therefore the terminal or emulation program should not locally display characters as they are sent.

Additional Hyperterminal settings that should be configured for best operation are shown in the following table:

Function, Arrow & Cntrl Keys act as:	Terminal
Backspace Key sends:	Ctrl+H
Emulation:	ANSI
Backscroll Buffer lines:	0

Table 3 – HyperTerminal Settings

A standard RS-232 modem interface cable between the RDS+ and the PC or terminal is used for console connectivity.

3.2.2 Start-Up and Session Initiation

Once connected, with the terminal or emulation program running and the RDS+ powered on, communication between the operator and the system is enabled.

Upon power-up of the system, the RDS+ outputs an initialization banner to the console, similar to the following:

```

-----
Network Delay Simulator Firmware Rev 0.6
      East Coast Datacom      Apr 18, 2005
-----
Initializing...Configuring Hardware...
Loading FPGA Image; neds_top.ncd 2s200fg256 2005/04/11 15:20:39

```

This banner message will appear on the screen for about 15 seconds while the system initializes, during which the SYS STATUS indicator on the front panel is illuminated yellow. At the end of this process if everything has proceeded normally, the SYS STATUS indicator is changed to green and the system will refresh the display with the Operator's Display Window top-level window, shown in Figure 3-1.

NOTE: If the console connection is made or the terminal emulation is brought up after the RDS+ system has been powered-up, the terminal window will not likely show any meaningful message activity until the operator sends an appropriate keystroke sequence to the system. If the system is operating correctly, pressing the <ESC> key is the most direct method to cause the system to refresh the display window.

The display window structure is depicted in Figure 3-1. The window is divided into two sections: a top half that shows a semi-graphical depiction of the state of the system, and a bottom half that includes the menus and operator configuration selections.

Menu choices are either options that lead to other menus that present additional choices, or are parameter options. The illustration displays the Top-Level System Menu that leads the user to all the major functions of the system.

```

000 0:36                NETWORK DELAY SIMULATOR
                PORT A EIA-530 DCE                Port B RS-422/449 DCE

    Clk 768 KHz                768 KHz Clk
Data -----> Data
Ctrl -----> Ctrl

    Clk 768 KHz                768 KHz Clk
Data <----- Data
Ctrl <----- Ctrl

TOP-LEVEL SYSTEM MENU
[1] - Configuration Save/Restore
[2] - Port Configuration
[3] - Clock Options
[4] - Data Path Delays
[5] - Error Insertion
[6] - BERT
[7] - Data Loop
[8] - LED Display
[9] - Help

                                Use F1 for HELP

```

Figure 3-1 – Display Screen w/Top-level menu

3.2.3 Operator's Display Window Status Area

The status area of the display window is where a summary of the configuration and real-time operating status is shown in a character-graphic format. The illustration of Figure 3-2 shows an example.

The intent with this display is to depict the two data paths running across the screen, with a pair of lines for each representing the data path and the control path, respectively. The two pairs of lines run in opposite directions, the top from left to right, and the bottom from right to left, to better represent the bi-directional flow between Port A (on the left) and Port B (on the right).

Along each path line, fields for the various configuration options are shown when they are enabled, and if a parameter is involved, the associated value. The placement of the field corresponds to the position in the data path that the function operates. For example, the delay buffer when enabled, precedes the error generator.

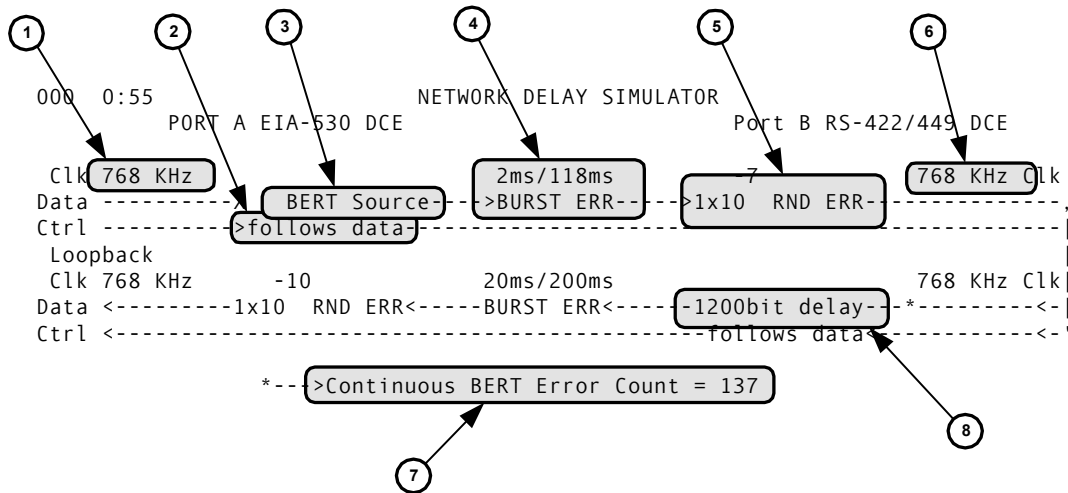


Figure 3-2 – Display Window Status Area

Referring to the above figure, fields in the status area that are varied altered according to the operating status of the system, are as follows

- 1) Clock rate, for the clock signal associated with Data
Appears at each data port, input and output (4 places)
- 2) Control signal delay enable status
Appears on each CTRL path when enabled (2 places)
- 3) BERT Pattern Generator insertion status (1 place)
Appears on either one of the DATA paths when enabled (2 places)
- 4) Burst Error generator enable status & parameter setting
Appears on each DATA path when enabled (2 places)
- 5) Random Error generator enable status & parameter setting
Appears on each DATA path when enabled (2 places)
- 6) Port Loopback Enable status
Appears on each DATA path when enabled (2 places)
- 7) BERT Pattern Checker
Appears on either one of the DATA paths when enabled (2 places)
- 8) Delay Buffer enable status & parameter setting
Appears on each DATA path when enabled (2 places)

3.2.4 Operator's Display Window Menu Area

In the operator menu area, the user has access to all features of the system and is able to make and put into effect RDS+ configuration changes. Additional features allow the user to store and retrieve up to 10 configurations.

3.2.5 Menu Screens and Navigation

The operator may move “down” from one menu to another by making menu selections, following the hierarchical flow, or may use certain control codes to move back “up” through the menus. The control codes are as follows:

<CTRL>T or Home– Return to the Top-Level System Menu

<CTRL>P or <ESC> – Return to the Previous menu in the hierarchy

Menu items are selected when a menu is presented, either by using the up/down arrow keys to move to the desired menu item, or by entering the number of the menu item. With either method the cursor appears to the left of the menu item selected.

Pressing the <ENTER> key while a menu item is selected will move the operator to the next menu screen, activate the function, or request additional information on the command line, depending on the context of the current menu item.

Three exceptions to the above are the Select Data Clocking Options menu item, the LED Display menu item, and the Help menu item. In all cases, invoking one of these options causes a multi-line informational display to replace the menu display. To return to the previous menu and exit the informational display, the <ESC> key must be pressed.

With the Select Data Clocking Options menu item, the informational display (character-graphic) allows configuration parameter changes to be made within the message area. Individual parameters are selected by using the TAB key to move sequentially through the clock parameters. Once a clock parameter is selected, a choice may be made from a list of parameter values by using the arrow keys, either up/down or right left, to obtain a desired value. Only when the <ENTER> key is pressed does the selected value take effect.

Function keys provide shortcut operations for certain menu items. These are:

F1 – Menu Help screen

F2 – Inject single bit-error on Path 1 (Port A to Port B)

F3 – Inject single bit-error on Path 2 (Port B to Port A)

F4 – Clear the BERT error counter to zero

3.2.5.1 Menu Tree

In the following sections the menu tree is presented as a series of hierarchical flow diagrams. Menu choices or options are shown as numbered boxes corresponding to the numbered list that appears in each menu.

Menu options shown as a five-sided box with a pointed bottom lead to another menu.

Menu options shown as a rectangular box are a final selection in the hierarchy. If nothing is below the box, this means the named action is invoked by hitting <ENTER> when the option is selected. If a line of text is displayed below the box, it indicates a command line response is needed to complete the operation.

3.2.5.2 Top-Level System Menu

This menu is shown below in Figure 3-3.

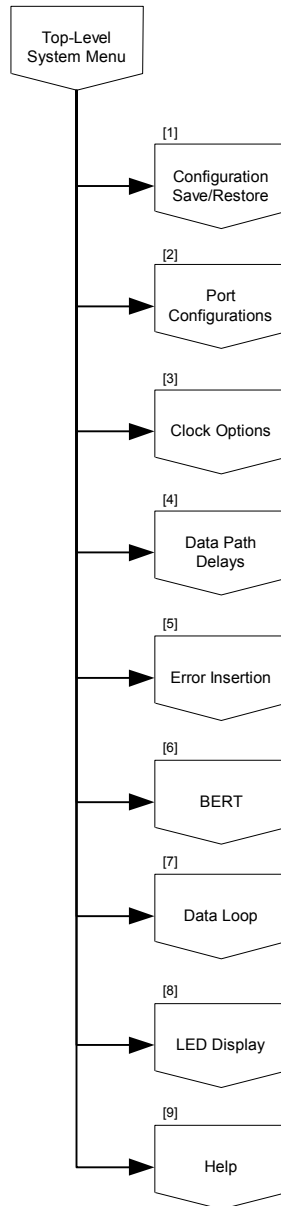


Figure 3-3 – Top Level System Menu

From the top-level menu several subsidiary menus may be chosen:

[1] Configuration Save/Restore – Allows the operator to store and retrieve configurations in a non-volatile section of memory. There are eight configuration memory locations, including one for automatic power-up retrieval.

[2] Port Configurations menu – Presents options for interface type and clocking independently for Port A and Port B.

[3] Clock Options menu – Provides Port A and Port B clocking options and system clock generation options.

[4] Data Path Delays – Allows the operator to control delays independently for Path 1 and Path 2 delay buffers.

[5] Error Insertion – Allows the operator to determine the parameters for the type and rate of random and burst errors independently on each data path.

[6] BERT – Provides a means to inject a BERT 511 pattern into either data path and/or selectively test for the same pattern on either data path.

[7] Data Loop – Allows setting up a loop function on the output of either data path in order to loop the same data back through the other path.

[8] LED Display – Presents a depiction of the ON/OFF state of the 16 LEDs on the front panel.

[9] Help – Provides useful information for function keys and menu navigation, including contact information for customer service.

3.2.5.3 Configuration Save/Restore

This menu is shown below in Figure 3-4.

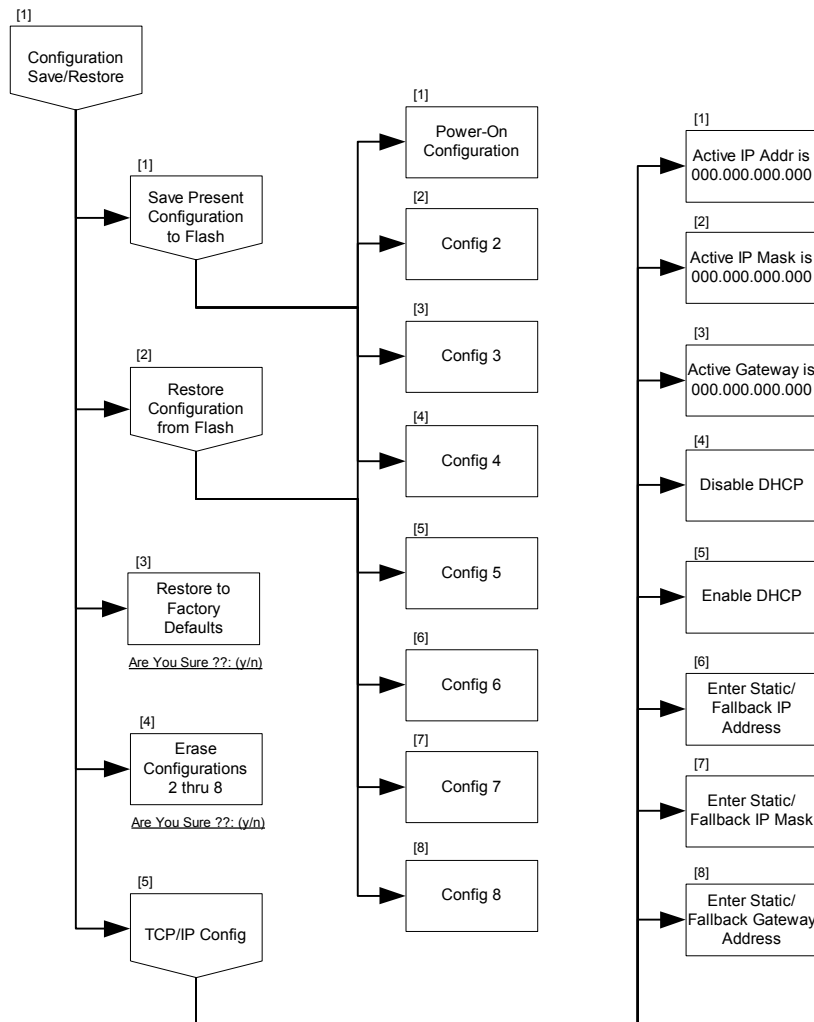


Figure 3-4 – Configuration Save/Restore Menu

3.2.5.4 Port Configuration

This menu is shown below in Figure 3-5.

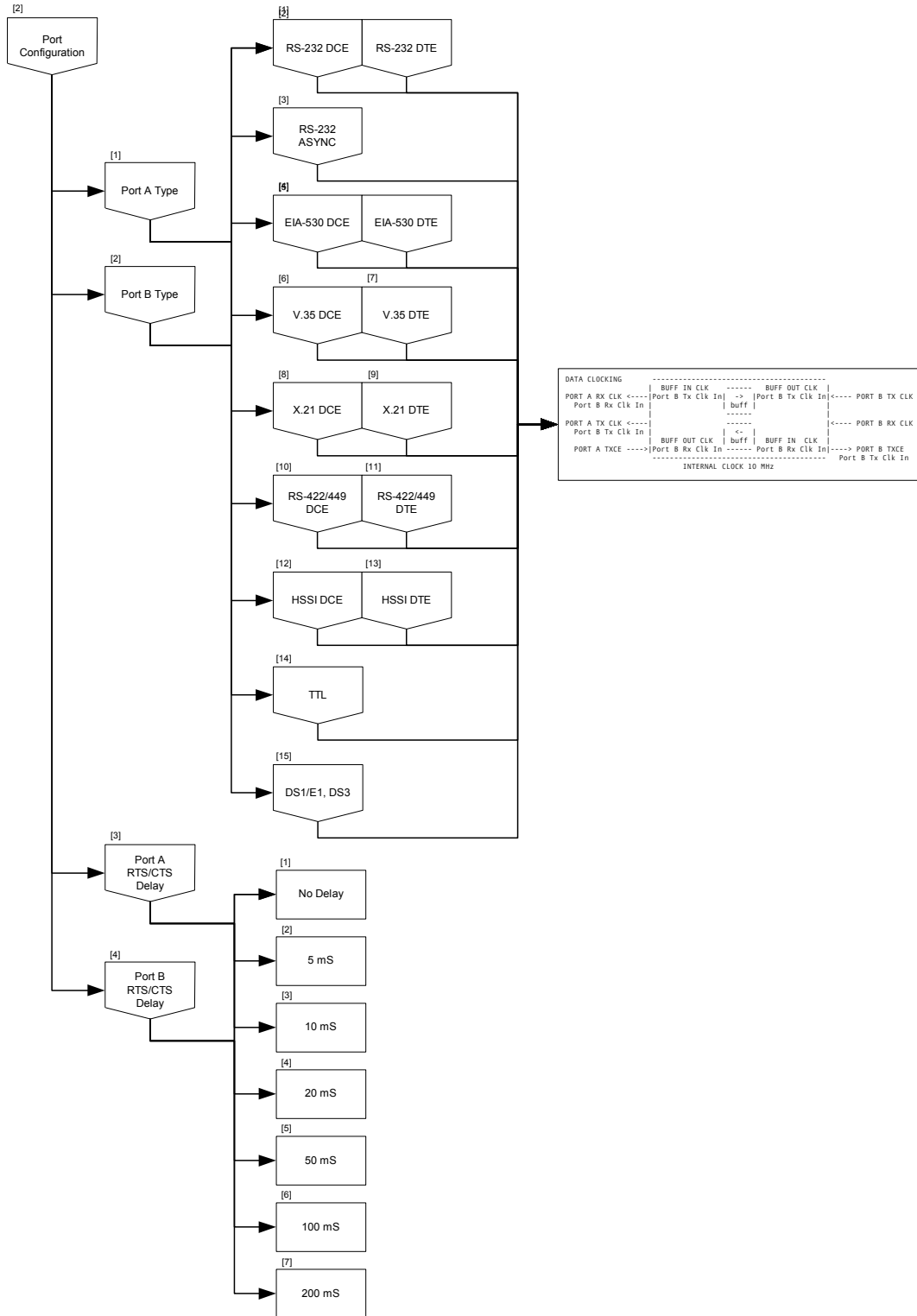


Figure 3-5 – System Configuration Menu

3.2.5.5 Clock Options

This menu is shown below in Figure 3-6.

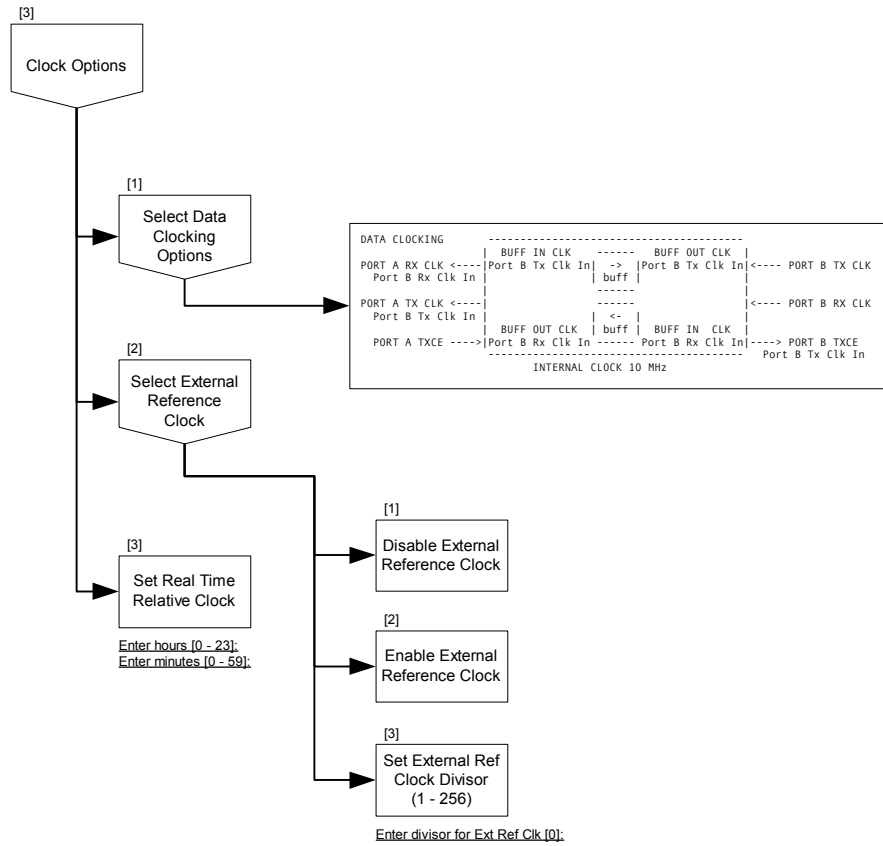


Figure 3-6 – Clock Options Menu

3.2.5.6 Data Path Delays

This menu is shown below in Figure 3-7.

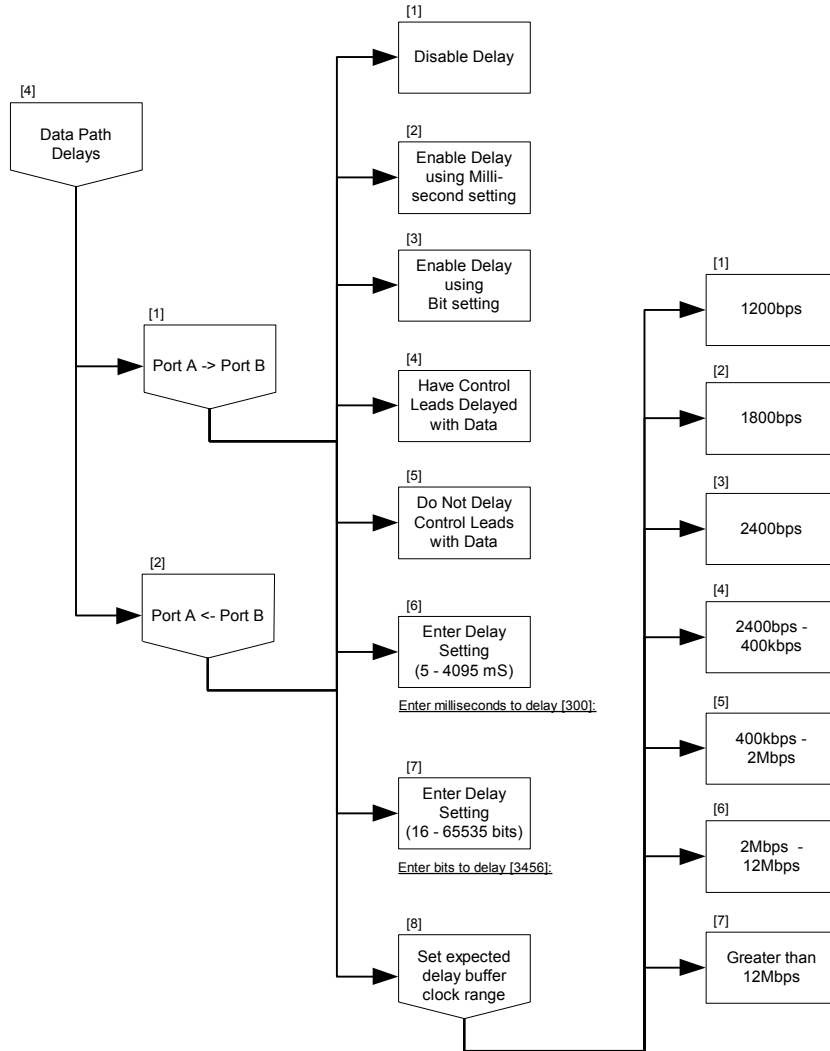


Figure 3-7 – Data Path Delays Menu

3.2.5.7 Error Insertion

This menu is shown below in Figure 3-8.

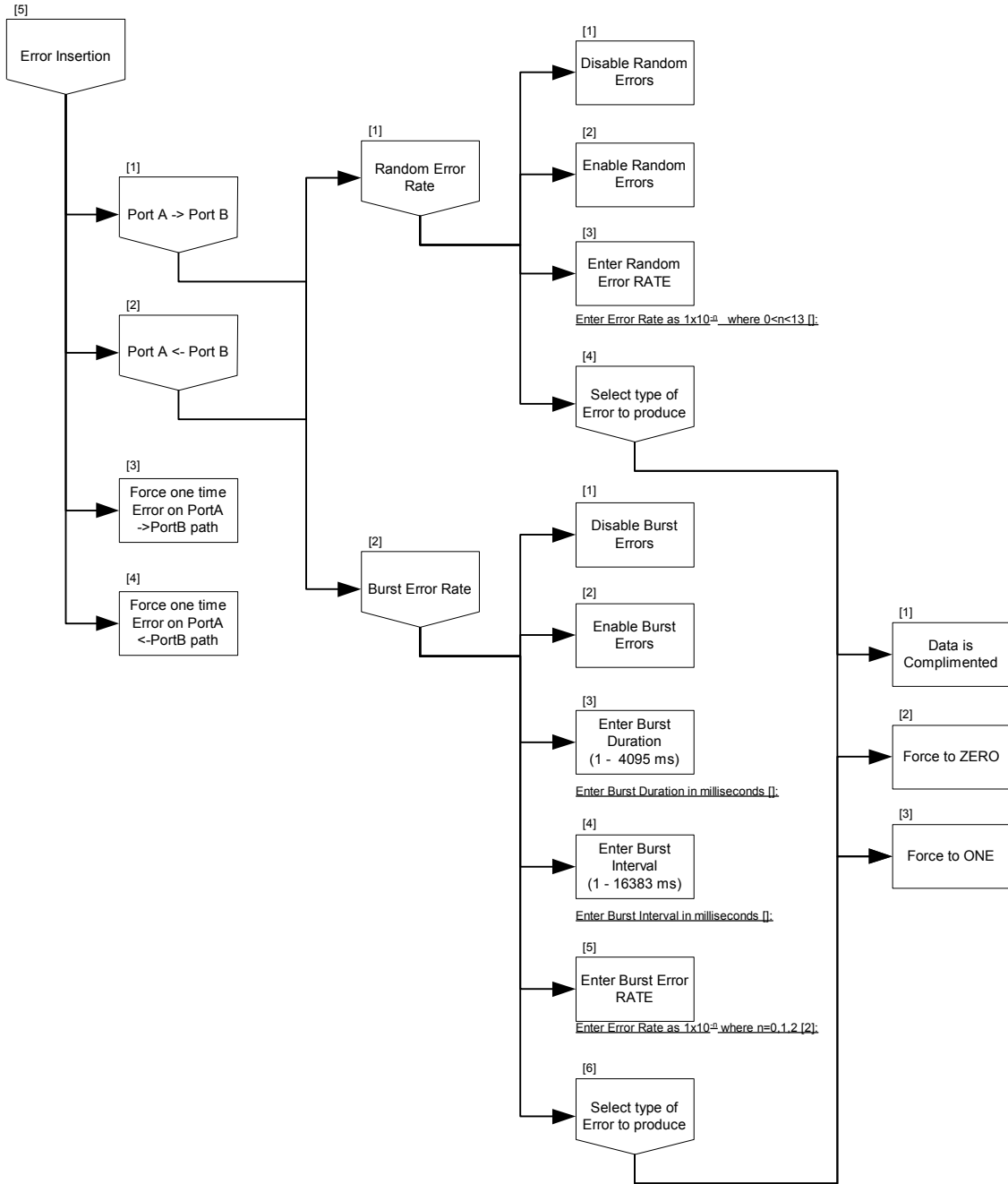


Figure 3-8 – Error Insertion Menu

3.2.5.8 BERT

This menu is shown below in Figure 3-9.

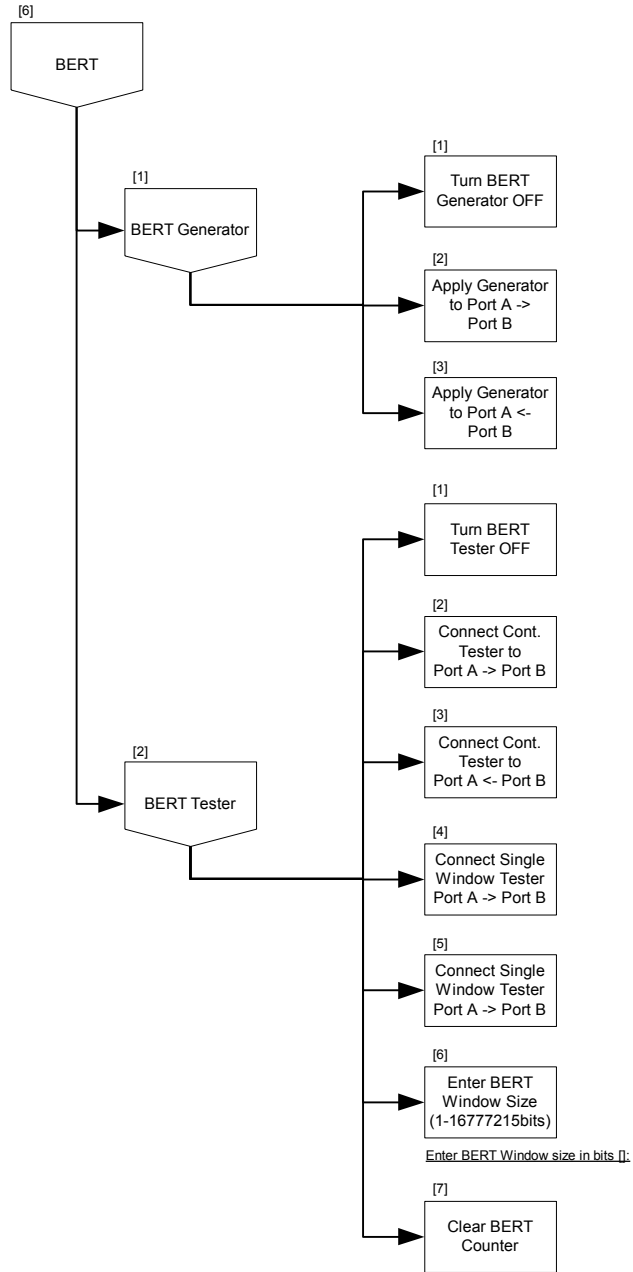


Figure 3-9 – BERT Menu

3.2.5.9 Data Loop

This menu is shown below in Figure 3-10.

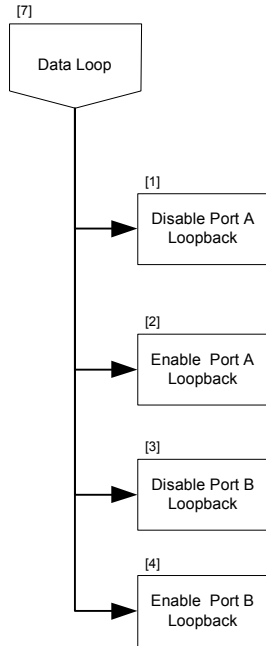


Figure 3-10 - Data Loop Menu

3.2.5.10 LED Display

This menu is shown below in Figure 3-11.

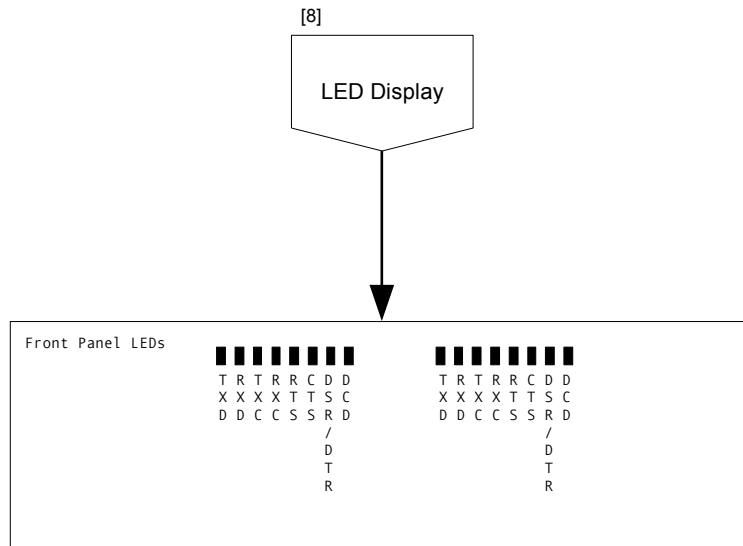


Figure 3-11 - LED Display

3.2.6 System Monitor Screen

The system monitor screen provides a means to perform system-related accesses, functions, and actions for a skilled operator or technician. This screen is not presented as an option on the system menus, and can only be reached via a particular set of keystrokes.

Currently, the only actions for which an operator has need to invoke the system monitor screen is to complete the process of downloading revised firmware modules into FLASH memory.

To access the system monitor screen the user must type: `<CTRL>ecd`. The set of three characters following the control key may be either uppercase or lowercase, and may be in any sequence. To leave the system monitor screen the user must type: "menu" or "MENU".

Once on the system monitor screen, the terminal window will display a ">" prompt at the beginning of each line, indicating that it is waiting for the next command to be entered.

3.2.6.1 Firmware Download Procedure

There are two types of firmware modules: **program** and **FPGA**. Each type of firmware module is downloaded as separate files, and it is not usually necessary to update both firmware modules at the same time.

Program and FPGA files have different file extensions; program files have a **.bin** extension, whereas FPGA files have a **.bit** extension. The user should understand which type of firmware file is being downloaded and the reason why a firmware update is needed.

In order to download the firmware files, a terminal emulation program which supports the 1Kxmodem file transfer protocol is required. The following procedure assumes the user utilizes the **HyperTerminal** emulation program installed on most Windows PC platforms.

Step 1:

After receiving the firmware download modules, make sure the appropriate file (either program or fpga) is in a known location, either on the system hard drive or other removable media. This location must be accessible from the terminal emulation program.

Invoke the system monitor program with `<CTRL>ecd`.

Step 2:

At the command prompt, type the following:

```
x1kr<Enter>
```

The command line will indicate that it is ready and waiting to begin accepting a file by generating this message followed by a string of characters about one second apart:

```
Initiate Xmodem1k Send  
CCCCC.....
```

(The waiting period will eventually time out after about 60 seconds. If it does so before the next step is completed, simply repeat this step.)

Step 3:

Center the mouse on the “Transfer” pull-down menu on the HyperTerminal menu bar. Click and move down to “Send File ...”.

A dialog box will appear requesting the filename, and the protocol. Browse to the appropriate directory and locate the appropriate .bin file to be downloaded and select “Open”. Make sure that 1KXModem is selected as the protocol.

Click on “Send”.

A window will appear showing the progress of the file download. When the file has been transmitted correctly to the Nx64-MUX, the command screen will display “Transmit Complete”.

Step 4:

This step will vary depending on whether the downloaded module is *program* or *fpga*.

At the prompt, type the following if the downloaded file is *program*:

```
prg <Enter>
```

Type the following if the downloaded file is *fpga*:

```
stfpga <Enter>
```

The Nx64-MUX will begin to store the firmware file into the appropriate sectors of FLASH reserved for the module, and should respond with a message similar to the following when completed. DO NOT attempt to interrupt the process or enter data until both of the following steps have been completed.

```
Erasing FPGA flash stores..done
```

```
Updating Flash...done
```

At this point the old firmware has been overwritten and the new revision has been installed. However, the new firmware will not be loaded into executable form until a system power cycle is completed.

Step 5:

With the firmware now safely stored in non-volatile memory, it is necessary to perform a system reset in order to load and start the new firmware program(s).

Perform a system reset by either,

- 1) Selecting *System Reset* on the System Functions Menu, or
- 2) Cycling the power to the system. This will cause the system to load from non-volatile memory, using the stored configuration.

3.3 HTML Browser Access via LAN

The RDS+ supports an optional LAN module to allow control and configuration of the unit via a Web Browser interface. When installed the LAN module ships from the factory with DHCP enabled. Therefore at power-on the RDS+ will request an IP address assignment from the local DHCP server. If DHCP is not desired then the LAN settings will have to be set using the ANSI Terminal Async console interface.

3.3.1 Getting Started

WITH DHCP ENABLED:

- 1) Insure the RDS+ is connected to the local LAN.
- 2) Power-on the RDS+.
- 3) Wait for the front panel SYS STATUS Led to light GREEN.
- 4) Give the RDS+ approximately 1 minute to negotiate an IP address.
- 5) Press the 'Push for IP Address' button on the RDS+ front panel.
 - This causes the display of the assigned IP address on the front panel Leds.
 - The IP address is displayed in the 'dotted' format (ie. 192.168.1.10), with only significant digits displayed (no leading zeros).
 - The IP address digits are displayed from left to right.
 - There is a 1 second begin phase where all Leds are off.
 - Each digit is represented by an equal number of Leds lit.
 - A zero digit is represented by only the TXD Led being lit.
 - The 'dot' is represented by all Leds being lit.
 - The end of the IP address display is noted by 1 second of all Leds off.
- 6) At any time during the IP address display the 'Push for IP Address' button can be pushed again to restart the address display sequence.
- 7) Bring up an Internet Browser.
- 8) Enter the RDS+ assigned IP address in the Address Bar of the Browser. Do not add www, use only the numeric address (ie. 192.168.1.10).
- 9) The RDS+ will paint the control page with the current configuration settings.

WITH DHCP DISABLED:

- 1) With DHCP disabled the RDS+ must be setup with static IP addressing.
- 2) Connect and turn on an ANSI Terminal (ie. Hyperterminal under MS Windows) to the serial 'ASYNC CONFIG' port on back of the RDS+. This terminal must be set up as:
 - 38400pbs.
 - 8,N,1 bits,parity,stop.
 - No flow control.
 - ANSI Terminal Emulation
- 3) Power On the RDS+.
- 4) Wait for the front panel SYS STATUS Led to light GREEN.
- 5) The main configuration menu screen will display.
- 6) Select menu item [1] Configuration Save/Restore by hitting the Enter key.
- 7) The Configuration menu will display.
- 8) Select menu item [5] TCP/IP Config buy hitting 5 then Enter.
- 9) The TCP/IP ADDRESSING menu will display, showing in BLUE highlight the current DHCP option set.
- 10) To disable DHCP hit 4 then Enter.
- 11) Now hit 6 then Enter and at the prompt at the screen bottom enter the desired static IP Address. Use the Enter key to set your choice.
- 12) Now hit 7 then Enter and at the prompt enter the desired IP Address Mask.
- 13) If a gateway router is to be used hit 8 then Enter and at the prompt enter the IP Address of the gateway.
- 14) Power down and back on the RDS+
- 15) Wait for the front panel SYS STATUS Led to light GREEN.
- 16) The RDS+ will now only be addressable by the static IP Address assigned above.
- 17) Bring up an Internet Browser.
- 18) Enter the RDS+ static address in the Address Bar of the Browser. Do not add www, use only the numeric address (ie. 192.168.1.10).
- 19) The RDS+ will paint the control page with the current configuration settings.

3.3.2 RDS+ Web Page Interface

The nature of a Browser Web Page interface is such that the Browser must always initiate a transaction. The RDS+, which is performing as a Server cannot independently or asynchronously send data to the Browser. Therefore the RDS+ Web Page will auto-update. The default period for this update is 5 seconds. This period can be changed via the selection box at the far bottom right of the page.

At any time the Browser REFRESH icon can be used to cause a complete page update.

The RDS+ Web Page is one elongated page that is logically divided into four main sections, and a few miscellaneous controls. The main sections are:

1. Top display area showing RDS+ front panel LEDS, what interface cards are 'installed', and what Config setting set is being used.
2. A BERT control box.
3. Two Data Path control boxes for setting the data path delays and error injections.
4. A Data Clock Source control area.

When using the BERT and Data Path control boxes a change to a setting does not 'take' until the Submit button is pushed. To aid the operator, the appropriate Submit button will change to RED text when it needs to be pushed for action. If the operator has a change of mind then the Cancel button will return the settings to their currently active values. The Submit button will remain RED until the RDS+ responds to the Browser, which means the action has taken place or the Cancel is complete.

For all settings other than BERT and Data Path control a complete page refresh will take place. This refresh will come in 'waves' and the operator must be cautious to insure that the refresh has completed entirely.

Appendix

A Questions, Common Problems and Helpful Tips

A.1 Differences between Simulated Delay and Real Delay

Communication systems rely on a transmission medium to propagate information signals from one point to another. Typically, this medium is either wire, fiber or free space. In all cases of signal propagation through these mediums, the signal is continuous, and is limited by a fixed speed, for example the speed of light.

There are other types of delay in networks that also contribute to end-to-end delay that are introduced by the equipment that attaches to or terminates network links. Usually the operator does not care what type of delay or the physics of propagation, but with a knowledge of how much data delay is expected, simply wants to create a realistic simulation.

Nevertheless, the user should be aware of the principle on which the RDS+ creates simulated delay in order to avoid false expectations about the results.

The RDS+ uses a storage buffer (a modified First-In, First-Out, or FIFO, memory) to hold the serialized received data before sending it out again after a delay period. There are two very important characteristics of the buffer that distinguish it from real-world propagation delay:

- 1) The buffer stores, and therefore delays only the data signal, and not the clock signal.
- 2) The buffer uses the clock signal to “sample” the data on each clock transition and stores one bit per clock.

In order to produce a simulated delay, the RDS+ begins by storing each sequential bit in the FIFO buffer. At the same time the delay simulation starts, a counter begins counting either time, or bits, depending on how the user has configured the system. At the end of the time (or bit count) period, the system locates the first bit stored and begins retrieving each sequential bit in the order it was stored.

For the time delay to remain constant, the clocks chosen to clock the buffer input and output must always be equal and constant in frequency from the time the simulation begins. If for example the output clock speeds up, the number of data bits in the FIFO will decrease with time until there is no delay, and will finally result in an underrun condition in which the serial data out is no longer the same as the serial data in.

Another example is if both clocks should change speed equally. In this case, the rate at which data is stored and retrieved changes, but equal for both input and output of the FIFO. Therefore, the number of bits held in the FIFO remains constant. However, since a bit is now defined by a longer or shorter clock period, the length of time these bits remain in the FIFO is altered. For example, increasing the clock frequency on both buffer input and output by 10%, decreases throughput delay by 10%, even while the bit number delay is constant.

As an exercise, the operator might consider this question: Starting with equal-rate buffer input and output clocks while operating with fixed delay, if the buffer input clock changes by some proportion, how much later should the output clock change by the same proportion in order to maintain the original delay? Hint: Think about what would happen if the input clock should stop.

A.2 Types of Working Configurations

A.2.1 Internal Clock Timing

Internal Clock Timing is normally used when both RDS+ interface cards are DCEs. In this configuration, clocks are sent from the RDS+ to both attached devices. The internal clock source is a Stratum 4 standard clock when it runs without an external timing source.

An external timing source may be used with the internal oscillator to frequency-lock the generated internal clocks to an external reference. The external reference must be a multiple of 8KHz, within 100 ppm of nominal frequency, up to a maximum of 2.048 Mbps.

A.2.2 Flow-through Clock Timing, Unidirectional and Bidirectional

Flow-through Timing allows one attached device to clock the RDS+, and to pass that clock timing to the other attached device. Typically, the RDS+ will have one DCE and one DTE to facilitate this configuration. In this application, the internal clock will not be used.

With the flexibility of assigning and routing interface clocks on the RDS+, the clock timing flow may be either bidirectional or unidirectional. Unidirectional works best when both cards are standard EIA-type interfaces, where one is a DTE and receives a transmit and receive data clock, and the other is a DCE which sends a transmit and receive data clock. In this case the timing flow is from DTE to DCE.

Bidirectional timing flow is usually associated with interface types that have a receive clock and a transmit clock that travel in the same direction as the corresponding data signal. This is typical of DS-1, DS-3, and the TTL Interface Card. Timing usually passes through the RDS+ in the same direction as the data. Since the data is bidirectional, then so is the clocking.

With bidirectional timing it is also not required that the two clock signals in opposing directions have the same frequency.

A.2.3 Independent Clock Timing

When both interface cards are DTE, then they both must accept timing from an attached device. It is possible to use the RDS+ in such a configuration, but it is important that the user must be able to insure that the separate clocks are timed to the same clock source, otherwise the delay buffer will not provide constant delay.

There are also applications where the RDS+ delay buffer may be used as an elastic storage buffer, where the two independent clock sources are timed differently. In this case the delay through the buffer is not constant, but variable over time.

A.3 Interfaces with Clock and Data Recovery (DS-1, E1, DS-3, E3, STS-1)

Most network interfaces combine timing and data over a single wire pair or optical fiber. The data transitions in the transmitted baseband signal offer the the receiver the means to recover and separate clock and data.

Two properties of this type of interface are: 1) clock source timing must be more precisely controlled within a narrow range of frequencies about the nominal frequency, and 2) the process of recovering the clock causes the receive clock periods to deviate slightly over time from the transmitted source clock.

The first property above means that in any configuration, careful attention must be paid to the clock source. A stratum 4 clock (32 ppm) is usually considered the basic minimum requirement for most telecom circuits. Only one such clock timing source is required, as long as the recovered clock is passed along and used for timing at the next interface or returned back to the source.

The second property means that a received clock must be expected to deviate in frequency for short intervals from the clock timing source. For the RDS-Plus, this means that if the buffer output clock from the box is not the same as the buffer input clock along the same data path, then the delay buffer must be used to prevent occasional bit errors. For most DS-1 and DS-3 interface, for example, a minimum programmed bit delay of about 40 bits will serve to absorb clock jitter and wander and yet provide as close to zero delay as practical.

The figure below illustrates two common configurations, one using a single “network”, or external timing source, and the other the internal RDSPlus timing. In Configuration A (the default configuration for DS-1, E1, DS-3, E3 and STS-1 interface selections), the RDSPlus passes timing along the data path from the input side of one interface to the output of the other. A common clock selection (RxCLK) is used for both input and output to the delay buffer, and allows the buffer to be completely bypassed without bit errors.

In Configuration B, the RDSPlus is the timing source and distributes this clock to the terminal devices and uses the same clock timing (see Note) to clock the buffer outputs. The terminal must use loop timing, meaning that the return path uses the recovered clock from the RDSPlus source. In this case due to the inherent jitter and wander of the recovered clocks, the delay buffer must be used as stated above.

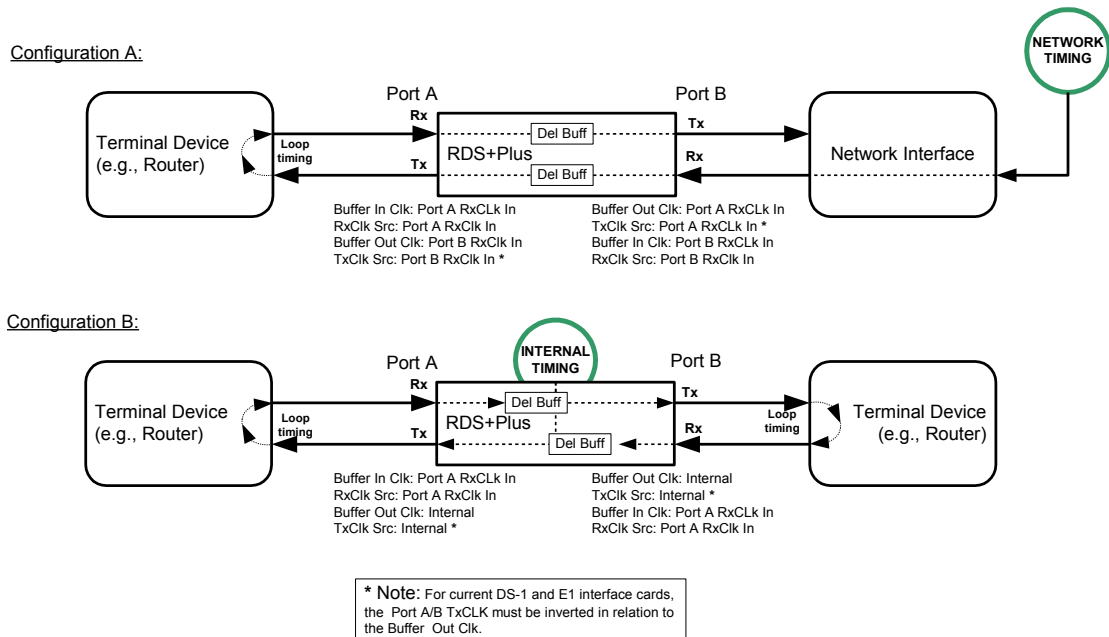


Figure A-1

B Port Interface Cards

B.1 Strapping Charts

Most of the Port Interface Cards have hardware straps that are normally set in a permanent position for the application where they are being used. The following tables list each user-configurable strap option for the listed cards.

RDS Interface Cards Strap Chart

VER 1.0
March 6, 2000

PT# 129014, RS-232 DCE Card

Jumper J2 Pos 1 - DSR is connected with other interface's DTR (if DCE) or DSR (if DTE) input
Pos 2 - DSR is forced on

Jumper J3 Pos 1 - DCD is connected with other interface's delayed RTS (if DCE) or DCD (if DTE) input
Pos 2 - DCD is forced on

Jumper J4 Pos 1 - RI is connected with other interface's RI (if DTE) input
Pos 2 - RI is unconnected (default if other interface is DCE)

PT# 129032, RS-232 DTE Card

Jumper J2 Pos 1 - DTR is connected with other interface's DTR (always DCE) input
Pos 2 - DTR is forced on

Jumper J3 Pos 1 - RTS is connected with other interface's delayed RTS (always DCE) input
Pos 2 - RTS is forced on

PT# 129012, RS-449 DCE Card

Jumper J2 Pos 1 - DM is connected with other interface's TR (if DCE) or DM (if DTE) input
Pos 2 - DM is forced on

Jumper J3 Pos 1 - RR is connected with other interface's delayed RS (if DCE) or RR (if DTE) input
Pos 2 - RR is forced on

Jumper J4 Pos 1 - TM is connected with other interface's TM (if DTE) input
Pos 2 - TM is unconnected (default if other interface is DCE)

Jumper J5 Pos 1 - IC is connected with other interface's IC (if DTE) input
Pos 2 - IC is unconnected (default if other interface is DCE)

PT# 129030, RS-449 DTE Card

Jumper J2 Pos 1 - TR is connected with other interface's TR (always DCE) input
Pos 2 - TR is forced on

Jumper J3 Pos 1 - RS is connected with other interface's delayed RTS (always DCE) input
Pos 2 - RS is forced on

PT# 129011, EIA 530 DCE Card

Jumper J2 Pos 1 - DSR is connected with other interface's DTR (if DCE) or DSR (if DTE) input
Pos 2 - DSR is forced on

Jumper J3 Pos 1 - DCD is connected with other interface's delayed RTS (if DCE) or DCD (if DTE) input
Pos 2 - DCD is forced on

Jumper J4 Pos 1 - TM is connected with other interface's TM (if DTE) input
Pos 2 - TM is unconnected (default if other interface is DCE)

PT# 129129, EIA 530 DTE Card

Jumper J2 Pos 1 - DTR is connected with other interface's DTR (always DCE) input
Pos 2 - DTR is forced on

Jumper J3 Pos 1 - RTS is connected with other interface's delayed RTS (always DCE) input
Pos 2 - RTS is forced on

PT# 129010, V.35 DCE Card

Jumper J3 Pos 1 - DSR is connected with other interface's DTR (if DCE) or DSR (if DTE) input
Pos 2 - DSR is forced on

Jumper J4 Pos 1 - DCD is connected with other interface's delayed RTS (if DCE) or DCD (if DTE) input
Pos 2 - DCD is forced on

Jumper J5 Pos 1 - RI is connected with other interface's RI (if DTE) input
Pos 2 - RI is unconnected (default if other interface is DCE)

PT# 129028, V.35 DTE Card

Jumper J3 Pos 1 - DTR is connected with other interface's DTR (always DCE) input
Pos 2 - DTR is forced on

Jumper J4 Pos 1 - RTS is connected with other interface's delayed RTS (always DCE) input
Pos 2 - RTS is forced on

PT# 129013, X.21 DCE Card

No Straps

PT# 129031, X.21 DTE Card

Jumper J2 Pos 1 - CONTROL is connected with other interface's CONTROL (always DCE) input
Pos 2 - CONTROL is forced on

C System Information

Technical Specification

Application

Interconnection of two devices, (e.g. terminal, modem, or other network or CPE with standard serial digital interfaces) located within proximity of each other while simulating network delays times, random errors, burst errors, and BERT capability

Timing

Timing Modes: Transparent (pass-through timing from one port to another with selectable routing); Internal (Stratum 4) clock synthesizer; Internal w/ frequency-lock to external Timing Port.

Port Capacity

Two Ports w/optional Interface Modules.

Data Format

Data transparent at all data rates. Async data over-sampled and buffered internally.

Data Rates

From 1200 bps to 51.84 Mbps

Delay Range

10 milliseconds(mS) to over 4000 mS, in 1 mS increments, or from 100 bits to over 65,000 bits in 1 bit increments.

Random Error Rates

From 1×10^{-1} to 1×10^{-12} .

Burst Error Rates

From 1×10^{-1} to 1×10^{-2} .

Burst Error Timing

On-interval from 1ms to 4 Seconds
Off-interval from 2ms to 16 Seconds

BERT

CCITT 511 Pattern generator and pattern checker. Counts errors

continuously, or in user-defined windowed periods. Counter is resettable on command or loss of Sync indicator.

Port I/O Interface Modules

RS-232, RS-422/449, RS-530, V.35, X.21, TTL, HSSI, DS1/E1, DS3, E3, STS-1.

Control Leads Passed

All control leads RTS, CTS, DSR, DCD, DTR, or equivalent, sensed and mapped port-to-port. RTS and CTS leads may be delayed with data when passed from port to port.

Indicators

Power, System Status, TX Data, RX Data, TX Clock, RX Clock, RTS, CTS, DCD, DSR, DTR.

Power Source

85-264 VAC @10%, 47-440 Hz, IEC Power Inlet, (2) 5mm Fuses.

Environmental

Operating Temp.....32° to 122° F
(0° to 50° C)
Relative Humidity.....5% to 95%
Non-Condensing
Altitude.....0 to 10,000 feet

Dimensions

Height 1.75 inches (1U - 13.32 cm)
Width 16.5 inches (41.9 cm)
Length 8.5 inches (21.6 cm)

Weight

2 pounds (.92 Kg)

Warranty

One Year, Return To Factory

Ordering Information

For further detailed technical information on this product, contact East Coast Datacom Technical Assistance toll free in the US at (800) 240-7948 or (321) 637-9922 or Email: info@ecdata.com

Part #: 175000

Model: RDS-PLUS, Base Unit

Description:
Router Delay Simulator-Plus

Optional Interface Modules:

129014	RS-232 DCE I/M
129032	RS-232 DTE I/M
129010	V.35 DCE I/M
129028	V.35 DTE I/M
129011	RS-530 DCE I/M
129029	RS-530 DTE I/M
129012	RS-422 DCE I/M
129030	RS-422 DTE I/M
129013	X.21 DCE I/M
129031	X.21 DTE I/M
129057	TTL I/M
151028	HSSI I/M
175020	DS3 I/M
175021	E3 I/M
175022	STS-1 I/M
175023	T-1 I/M
175024	E-1 I/M
175025	10base-T LAN I/M